DICK SMITH SYSTEM 80

Technical Manual

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DICK SMITH

SYSTEM 80

Technical Manual

Preface

This manual is intended to provide owners of the Dick Smith System 80 with additional information to assist the understanding of operation and to facilitate easy repair should this be necessary.

In this manual, the operation inside each functional block is described. Troubleshooting flowcharts are provided, however, these flowcharts should be treated as guides rather than rules.

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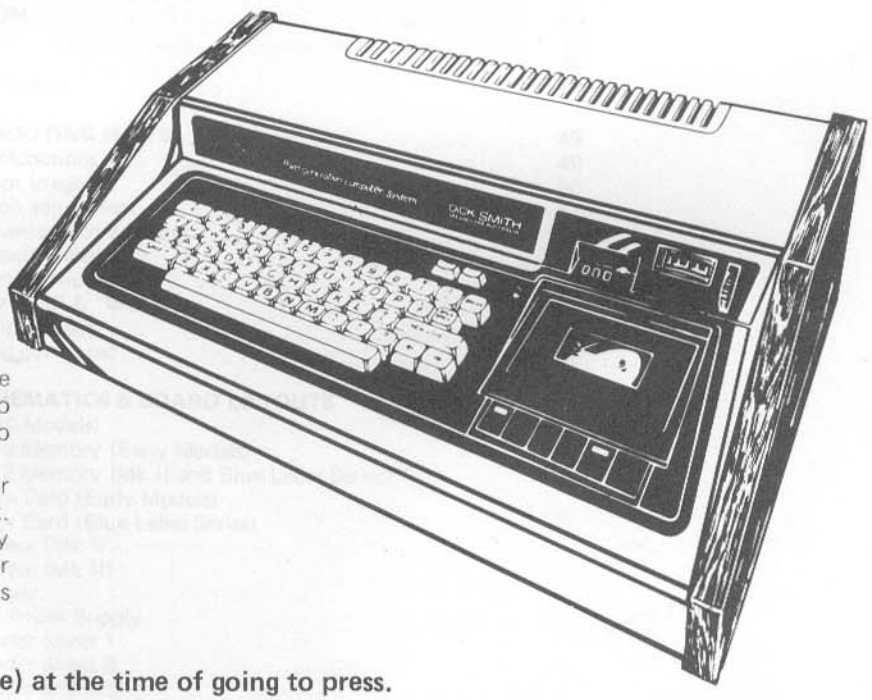

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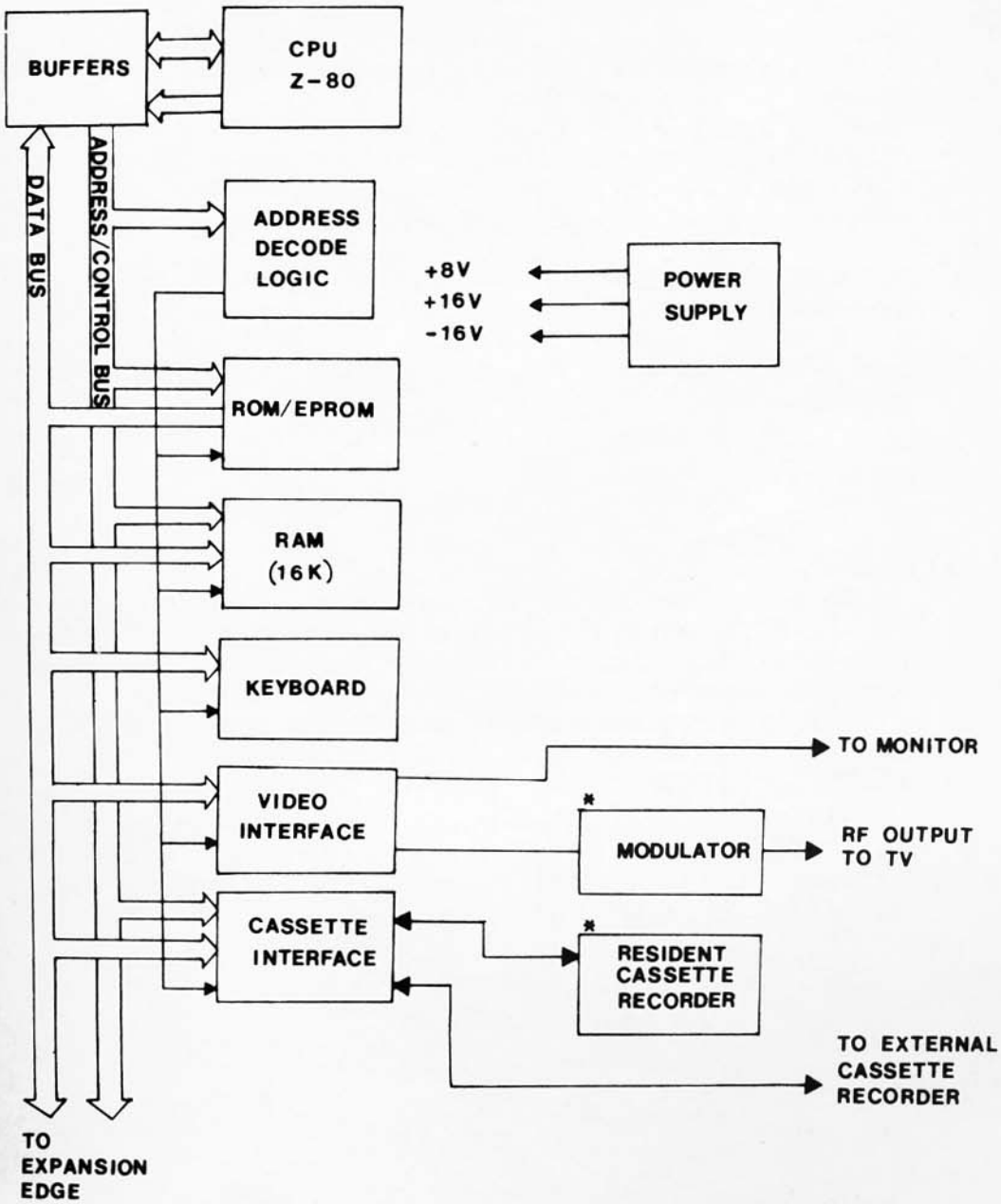
1. THEORY OF OPERATION

The hardware of the System-80 is described one-by-one in this section. The Computer consists of the following functional blocks: CPU, system ROM, user RAM, address decode and buffers, video interface, cassette interface, keyboard and power supply. These blocks are generally common to both MKI and MKII, and the differences will be mentioned in the appropriate sections. See Fig. 1.1 on system blocks.

Fig. 1.1 SYSTEM BLOCK DIAGRAM



* NOTE: This is absent in the MKII.

1.1 CPU

Z-80 is employed as the CPU chip which is an 8-bit N-channel microprocessor with 16 address lines. This 40-pin LSI requires single +5V DC supply. It provides 158 software instructions including those of 8080A CPU. Details refer to the data sheet of Z-80 in the appendix and the technical manual of Z-80.

1.1.1 Clock

The CPU operates at 1.7 MHz, derived from a crystal oscillator of either 10.644 MHz or 10.48 MHz and a divide-by-six counter, Z38. The oscillator is implemented on the interface board with three inverters of Z31 and a crystal.

1.1.2 Reset

Power-on reset and system reset are provided for proper operation of the computer. Power-on reset is achieved by a RC delay circuit. Initially, the capacitor C2 is discharged through a diode D1 as +5V DC is turned OFF. Once +5V DC is switched ON, C2 will slowly be charged up towards +5V. Pin 26 of Z-80 will experience a logic LOW as Vcc of the CPU has reached the operating supply voltage. Then, the CPU will be initialized with program counter set at ØØØØH.

System reset is done by pulling LOW the input of $\overline{\text{NMI}}$ (pin 17 of Z-80). As $\overline{\text{NMI}}$ (non-maskable interrrupt) is active LOW, the CPU will re-start execution at location ØØ66H without altering the programs stored in memory. The system reset button is present on the back panel . A capacitor C1 is added across the switch to minimize the switch bounce.

1.1.3 Buses

The bi-directional data lines from the CPU are immediately buffered by Z18, Z19, and Z20 (74L367). The input buffers are enabled when either $\overline{\text{M1}}$ or $\overline{\text{RD}}$ is active LOW during op code fetch, interrupt acknowledge, memory read or input cycles. The output buffers are disabled when the control signal, $\overline{\text{ADDBS}}/\overline{\text{DODBS}}$ is LOW.

The 16 unidirectional address lines are also buffered by Z4, Z6 and Z17 (74LS367). These address lines can be isolated from the system bus by pulling $\overline{\text{ADDBS}}/\overline{\text{DODBS}}$ LOW.

The control lines for read/write and input/output are buffered by Z16 (74LS367), and are decoded by Z15 to get memory read/write ($\overline{\text{MRD}}$ and $\overline{\text{MWR}}$) and port input/output ($\overline{\text{IN}}$ and $\overline{\text{OUT}}$) control signals. These control lines can be disabled by making $\overline{\text{C}}/\overline{\text{CDBS}}/\overline{\text{STADBS}}$ LOW.

1.1.4 Address Decode

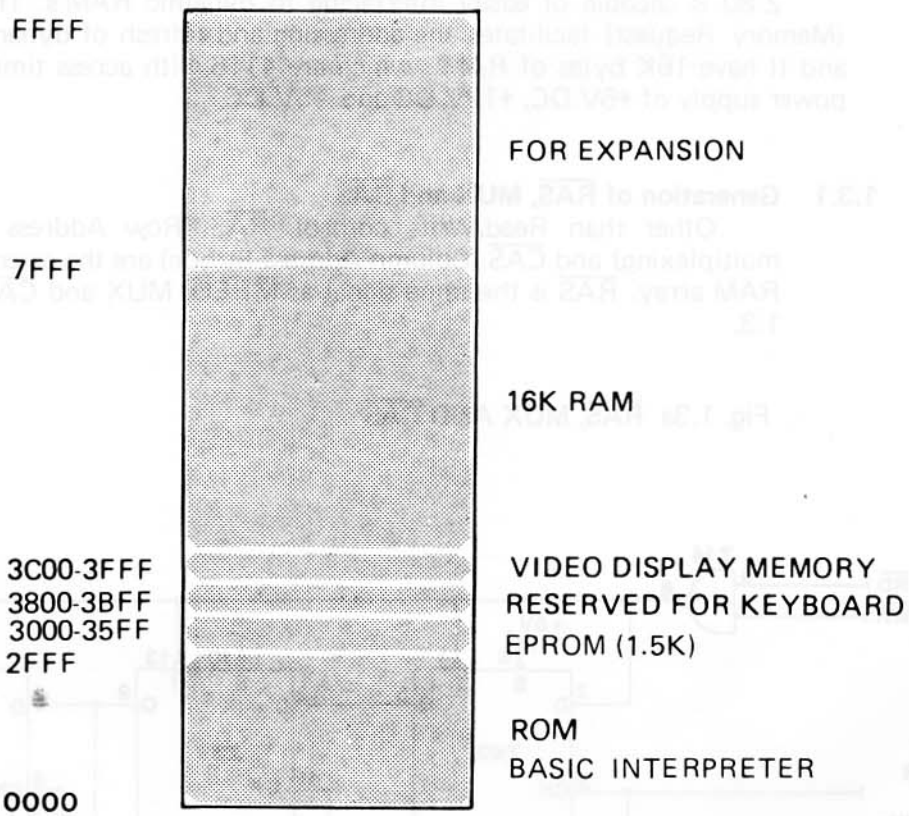
The address decode logic enables the CPU to access ROM, RAM, keyboard and video interface respectively. The logic is formed by Z22, Z25, Z35 and Z21. The decode scheme is illustrated as follows:

A15	A14	A13	A12	A11	A10	ENABLE	DECODED OUTPUT
0	0	0	0	X	X	ROM1 (Z10)	Z22 pin 9, 10
0	0	0	1	X	X	ROM 2 (Z11)	Z22 pin 11, 12
0	0	1	0	X	X	ROM3 (Z12)	Z22 pin 6, 7
0	0	1	1	0	X	EPROM (Z13)	Z22 pin 5
0	0	1	1	1	0	Keyboard	Z35 pin 11
0	0	1	1	1	1	Video RAM	Z35 pin 3
0	1	X	X	X	X	16K RAM	Z35 Pin 11.

Note: X means don't care.

Fig. 1.2 MEMORY MAP

MEMORY MAP



I/O PORT ASSIGNMENT

CASSETTE INTERFACE – FF, FE
PRINTER INTERFACE – FD

1.2 ROM

All System-80 computers have 12K bytes of Microsoft Extended BASIC interpreter stored in three 4K x 8 ROM's, E3001, E3002 and E3003. These ROM's are pin-compatible to standard 4K x 8 ROM chips. There is a 2K x 8 EPROM (2716) providing some special routines. In the Blue label computers the extended functions include upper case and lower case characters, flashing cursor, auto-repeat keyboard, screen print, machine language monitor and renumbering. It occupies 1.5K bytes of the EPROM.

In the MKII computer, besides the upper case and lower case characters, auto-repeat keys, flashing cursor and screen print functions, the extra routines provide two more features. They are a dumb terminal, HOST communication, and RS232 communication routines. These routines occupy 1.5K bytes of the EPROM. How to use these routines is detailed in the User's manual.

The ROM's and EPROM share the data buffers (Z9) with the user RAM's. Z25 gives proper chip selection signals to these ROM's. When the ROM and EPROM are addressed, pin 11 of Z25 will be logic HIGH and disable the RAM select signal, $\overline{CAS}$ from Z37 pin 13. Conversely when the RAM's are addressed, pin 12 of Z25 becomes logic HIGH and pin 11 of Z25 logic LOW, that is, the ROM select decoder, Z22 is disabled.

1.3 RAM

Z-80 is capable of easily interfacing to dynamic RAM's. The control signal, $\overline{MREQ}$ (Memory Request) facilitates the addressing and refresh of dynamic RAM. Both GENIE I and II have 16K bytes of RAM's which are 4116 with access time of 250 nsec. They need power supply of +5V DC, +12V DC and −5V DC.

1.3.1 Generation of $\overline{RAS}$, MUX and $\overline{CAS}$

Other than Read/Write control, $\overline{RAS}$ (Row Address Strobe), MUX (Address multiplexing) and $\overline{CAS}$ (Column Address Strobe) are the essential control signals to the RAM array. $\overline{RAS}$ is the same signal as $\overline{MREQ}$. MUX and $\overline{CAS}$ are generated as in Fig. 1.3.

Fig. 1.3a $\overline{RAS}$, MUX AND $\overline{CAS}$

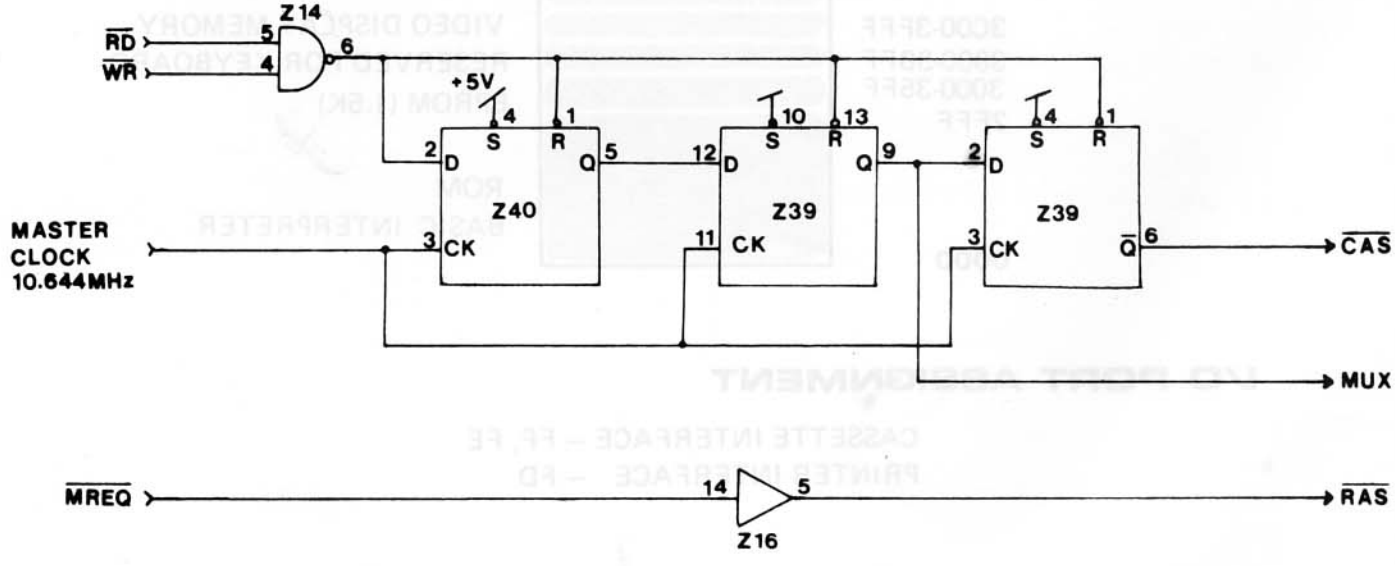
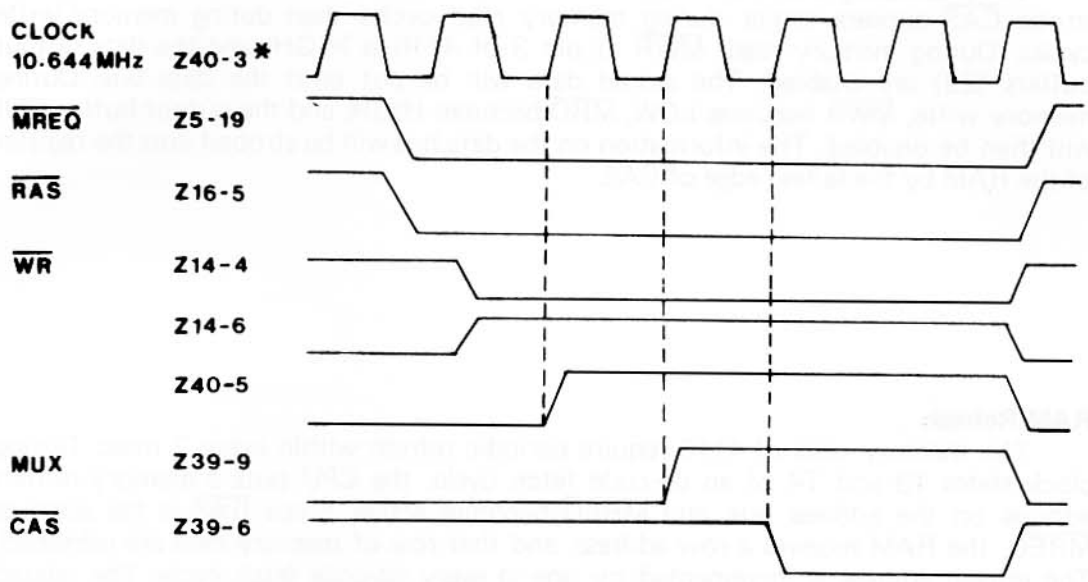


Fig. 1.3b TIMINGS OF $\overline{RAS}$, MUX AND $\overline{CAS}$



*NOTE: Z40-3 means pin 3 of Z40.

The generation of MUX and $\overline{CAS}$ is initiated and terminated by the $\overline{WR}$ or $\overline{RD}$ timing (Z14), and the active pulse width is determined by the time period of the master clock. When either $\overline{RD}$ or $\overline{WR}$ is active LOW, Z14-6 and Z40-2 will encounter a logic HIGH, and the D-type F/F (Z40-5) will change state from Ø to 1 upon the rising edge of the CLOCK. Then, MUX and $\overline{CAS}$ will become active at the following clocking edges respectively as shown in Fig. 1.3b.

1.3.2 Memory Read/Write

Since the RAM 4116 has internal row/column address latches, the address lines to the RAM are multiplexed by Z23 and Z24 (74LS157), and are controlled by the signal MUX. The row (or low order) address will appear on the address inputs of the RAM as MUX is LOW, and will be latched into the RAM by $\overline{RAS}$. As MUX is HIGH, the column (or high order) address appear on the address inputs of the RAM, and will be latched into the RAM by $\overline{CAS}$.

The addressing is similar in case of memory read and memory write although the strobe $\overline{CAS}$ appears earlier during memory read cycles than during memory write cycles. During memory read, $\overline{MWR}$ at pin 3 of 4116 is HIGH, and the data output buffers (Z9) are enabled. The stored data will be put onto the data bus. During memory write, $\overline{MWR}$ becomes LOW, $\overline{MRD}$ becomes HIGH, and the output buffer (Z9) will then be disabled. The information on the data bus will be strobed into the register of the RAM by the falling edge of $\overline{CAS}$.

1.3.3 RAM Refresh

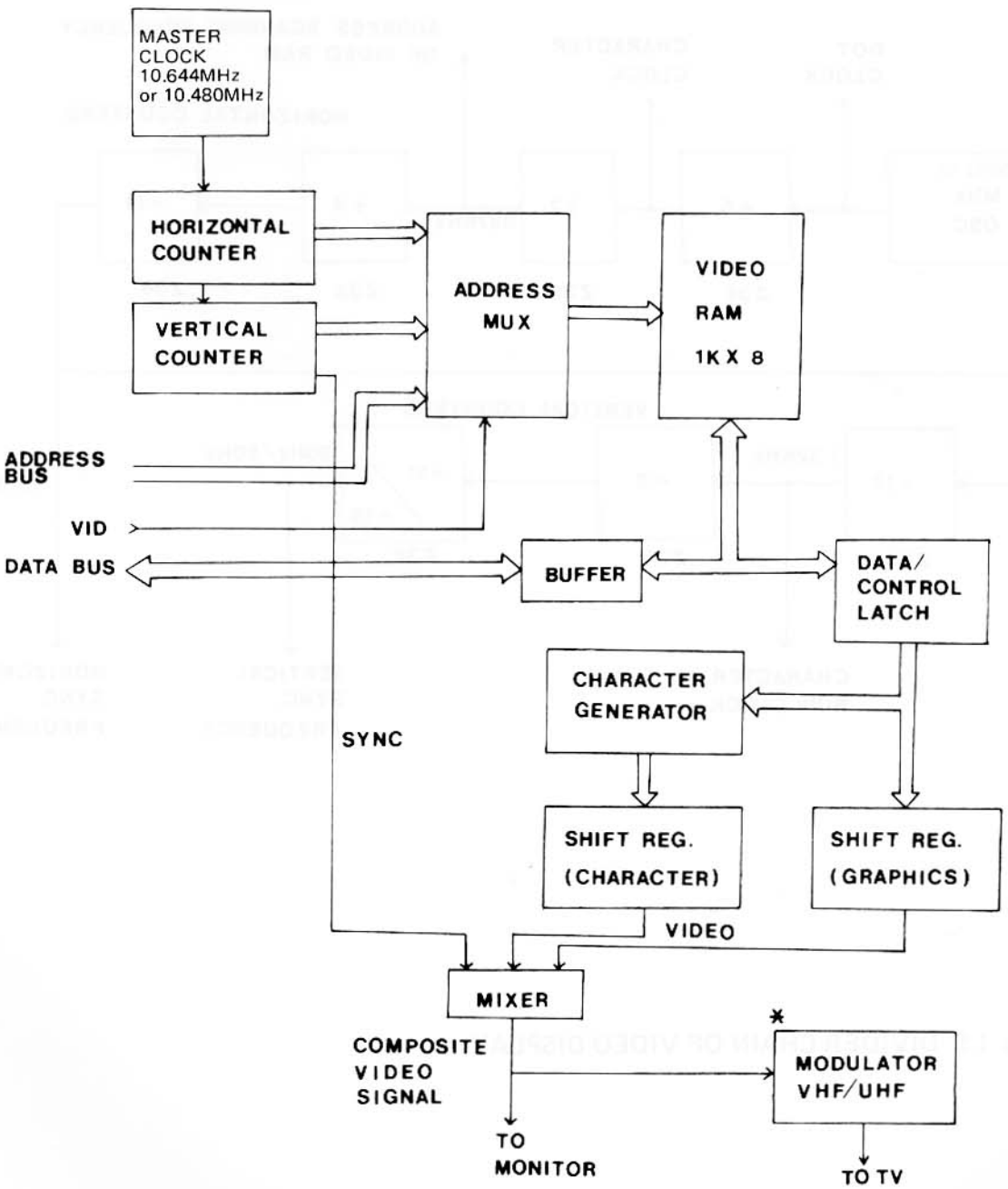
The memory cells of 4116 require periodic refresh within every 2 msec. During clock states T3 and T4 of an op-code fetch cycle, the CPU puts a memory refresh address on the address bus, and $\overline{MREQ}$ becomes active. Since $\overline{RAS}$ is the same as $\overline{MREQ}$, the RAM receives a row address, and that row of memory cells are refreshed. The refresh address is incremented by one in every op-code fetch cycle. The related timings are referred to the Z-80 data sheet in the appendix.

1.4 VIDEO INTERFACE

This section will reveal how the horizontal and vertical synchronization signals, and how the video signals are generated. In addition, we shall discuss how the video RAM's are accessed by the CPU, and are used to store the information displayed on a screen.

The structure of the video interface is illustrated in the block diagram of Fig. 1.4. It will be detailed in the following sub-sections.

Fig. 1.4 BLOCK DIAGRAM OF THE VIDEO INTERFACE



* NOTE: Not present in MKII computers.

1.4.1 Horizontal and Vertical Sync Signals

These two sync signals are generated by a divider chain with master clock of 10.644 MHz. The format of 64 characters/row x 16 rows is assumed in the following sections. Z36, Z35 and Z34 are the horizontal counters, and Z33 and Z32 are the vertical counters. The divider chain is shown in Fig. 1.5. Note that a character or a graphic unit is inside a 6 x 12 dot matrix.

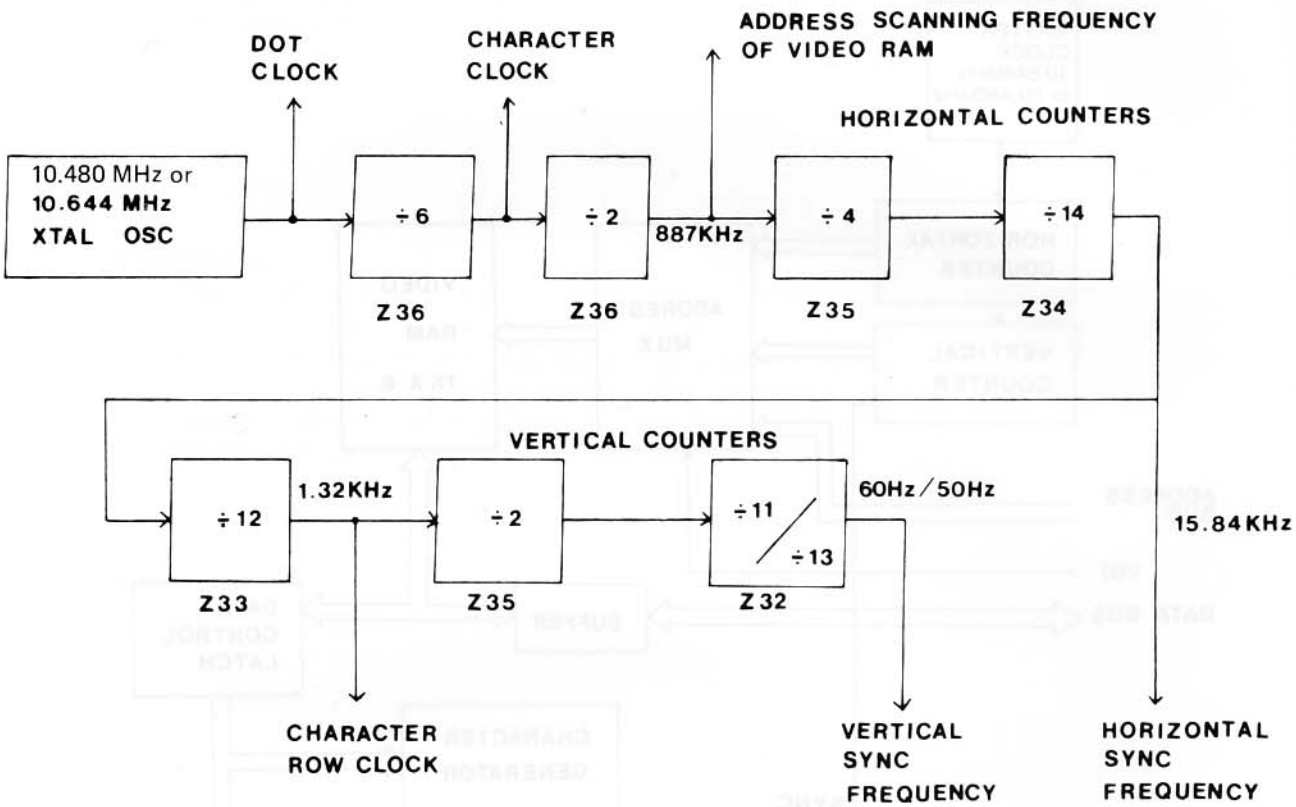
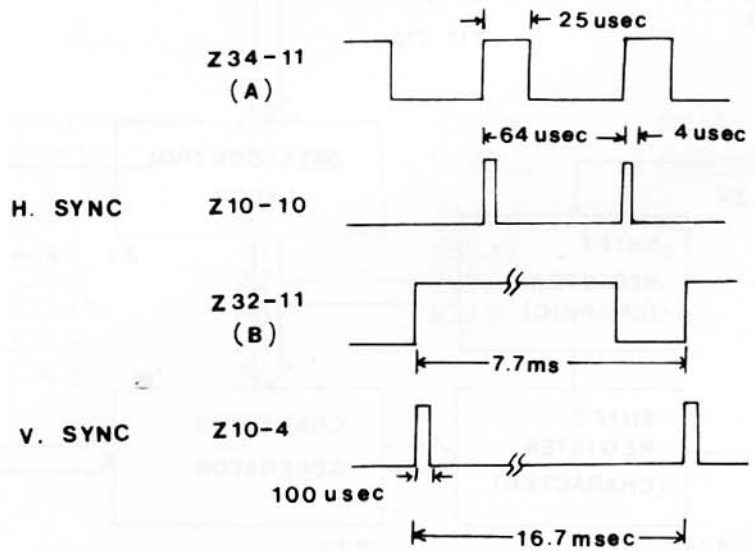


Fig. 1.5 DIVIDER CHAIN OF VIDEO DISPLAY

The outputs at Z34 – 11 and Z32 – 11 are the horizontal and the vertical sync frequencies (15.84 KHz and 50/60 Hz) respectively. These two sync frequencies will be shaped into the required sync pulses to a video display unit. First, VR1, C17 and four inverters (4069) delay the horizontal sync clock from Z34, while VR2, C16 and four inverters delay the vertical sync clock from Z32. Hence, we can shift the picture position by adjusting VR1 and VR2. Then, the two delayed signals are separately shaped into the desired sync pulses by a monostable circuit which contains a RC differentiating network and two inverters. The two sync pulses are shown in Fig. 1.6 Z22 forms an exclusive-OR gate, and sums up the horizontal and vertical sync pulses into the composite sync signal which is then fed to the video mixer to generate the composite video signal. (See section 1.4.3. on composite video signal).

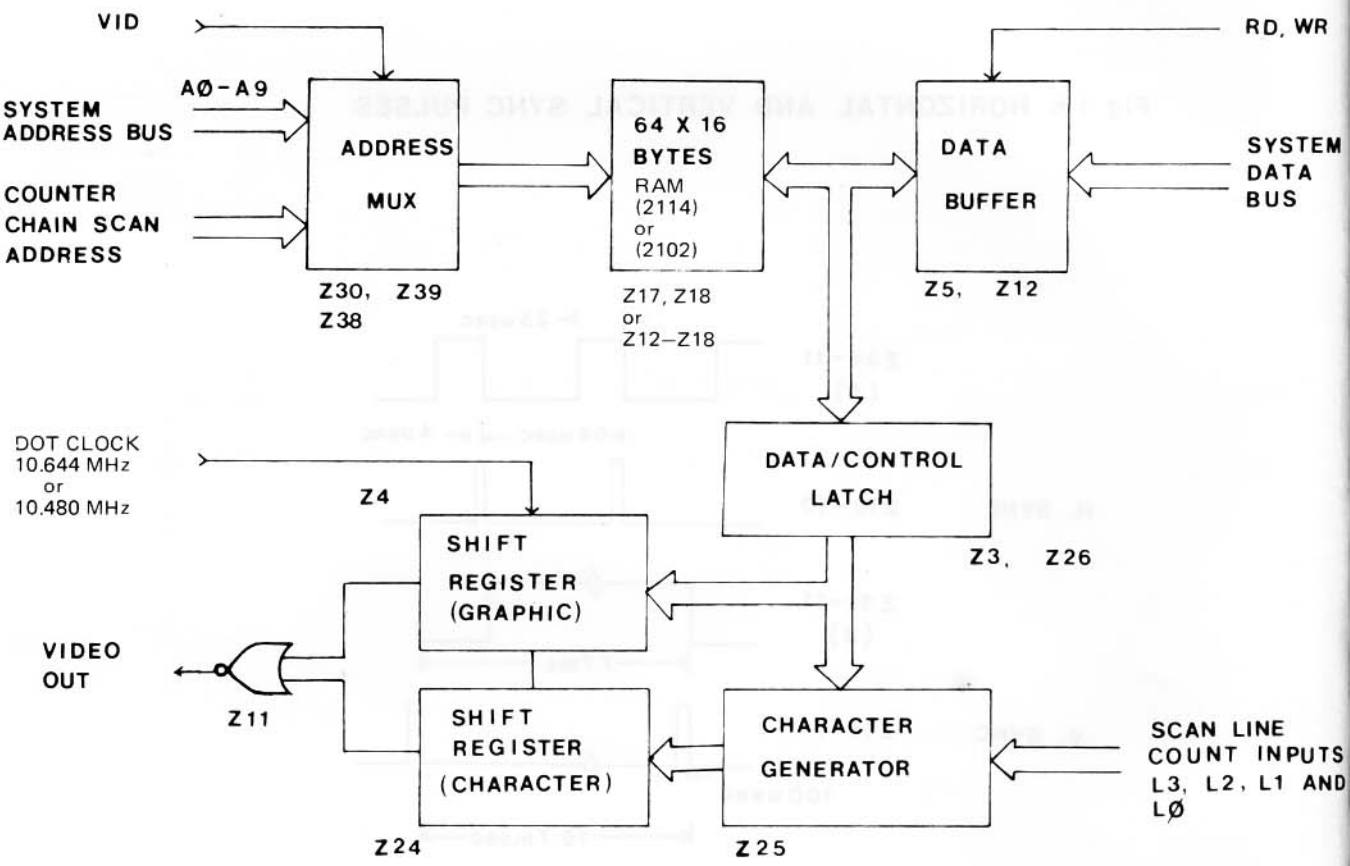
Fig. 1.6 **HORIZONTAL AND VERTICAL SYNC PULSES**



1.4.2 Video Memory

The video memory stores up the video information displayed on the screen. The memory is composed of two 2114 RAMS or, in older models, seven or eight 2102 RAMS.

Fig. 1.7 VIDEO RAM INTERFACING



1.4.2.1 Video RAM Addressing

The video RAM are addressed by either the CPU or the counter chain. In order to display a character at a certain position on the screen, the CPU has to write the ASCII code of the character into the corresponding location of the video RAM. The video RAM has address bits, A0 – A9 in which A0 – A5 specify one of the 16 rows. The 64 x 16 characters are memory mapped onto the 64 x 16 locations of the video RAM.

As the CPU is going to access the video RAM (3CØØH – 3FFFH), the address decoded signal, VID from the CPU board will be LOW. The address multiplexers Z30, Z39 and Z38 switch to the system address bus. At the write mode, the $\overline{WR}$ signal will set the RAM's $\overline{W}$/R line LOW and enable the input buffers, and then the data on the data bus will be stored into the RAM. At the read mode, the $\overline{RD}$ signal enables the output buffers, and the RAM will put the addressed data onto the data bus. Notice that the display is blanked during the CPU's access to the video RAM because VID sets the data/control latch Z3 and Z26 to the CLEAR state through Z40-6.

It is required to maintain a continuous display of information on the screen so that the video RAM will be scanned periodically by the counter chain. 64 video memory locations are read in sequence during the scanning of each line. Each row of characters occupies 12 scanning lines, and therefore, the vertical address increases by one every 12 lines. The outputs of the counters are connected to the RAM's address inputs through multiplexers Z29, Z30, Z37, Z39 and Z38. They are listed as below:

Horizontal Count	RAM Address	Vertical Count	RAM Address
Z36-8	A0	Z32-14	A6
Z35-9	A1	Z32-12	A7
Z35-8	A2	Z32-9	A8
Z34-12	A3	Z32-8	A9
Z34-9	A4		
Z34-8	Z5		

1.4.2.2 Video Signal Generation

In alphanumeric mode, the character generator is the essential part in producing the video signals. The character generator is MM52116 FDW (or custom chip, E3004) which provides upper case and lower case characters in a 5 x 9 dot matrix. Recall that each row of characters is composed of 12 scanning lines. The line count signals L3, L2, L1 and L0 of the character generator come from pin 11, 8, 9 and 12 of Z33 respectively. Z33 is the divide-by 12 vertical counter.

D7 of a character data is zero whereas that of a graphic data is one. As the video RAM is addressed by the counter chain, Z17 and Z18 (2114) are set to the READ mode. The ASCII code of a character from the RAM's are latched into Z26 and Z3 at the rising edge of the strobe at Z28-3. See Fig. 1.8(a). The character generator, Z25 is addressed by the six data bits from the latches, Z26 and Z3. The character generator will output the corresponding 5-bit dot signals of the character on the scanning line defined by L3-L0. When Z36 counts to 5, Z28-3 will be LOW, and then Z2-6 will also be LOW. The outputs of the character generator will be loaded in parallel into the shift register Z24. When Z28-3 becomes HIGH again, the dot signals will be shifted out serially from Z24-13 at the rate of the dot clock 10.644 MHz. Meanwhile, during the rising edge of the strobe at Z28-3, the next character will be latched into Z26 and Z3, ready for being shifted out next.

Fig. 1.8(a) VIDEO DISPLAY TIMING OF A CHARACTER

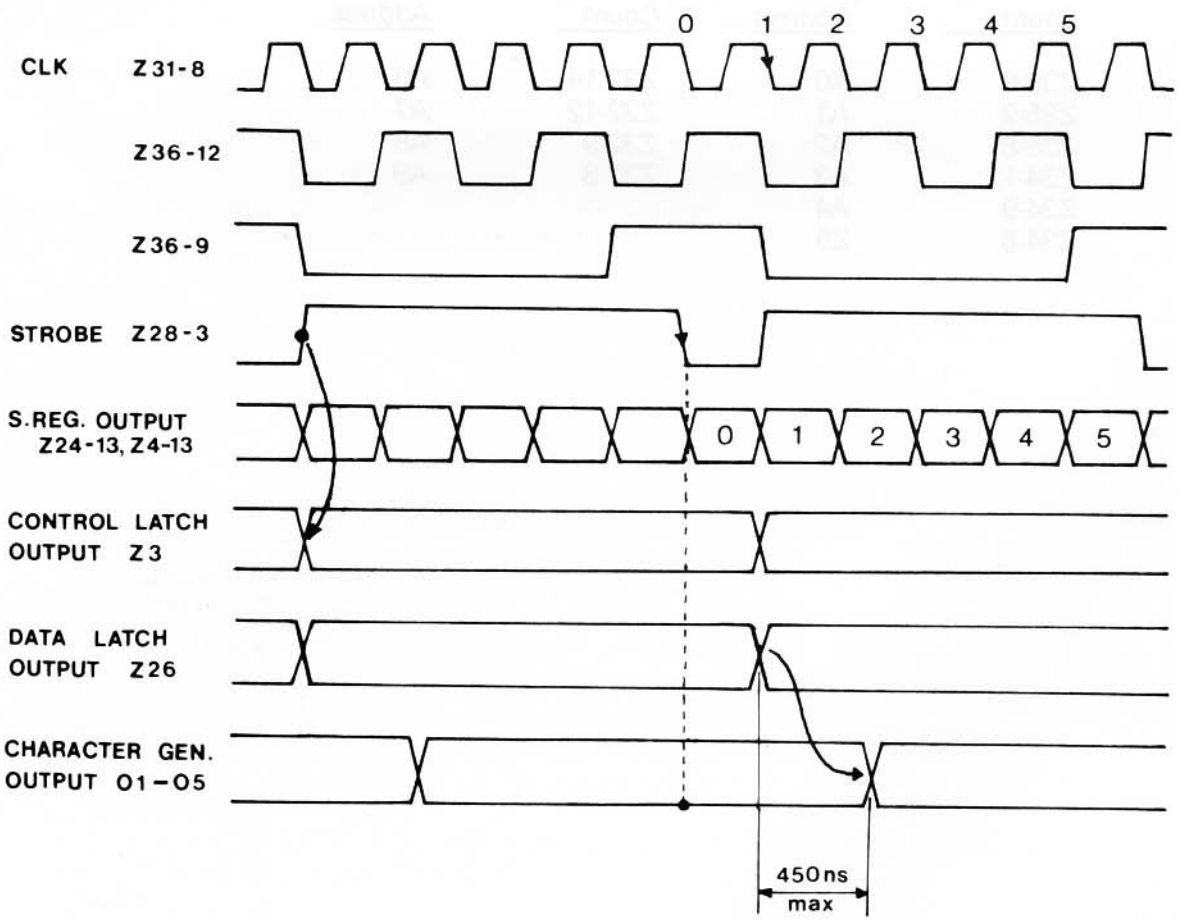
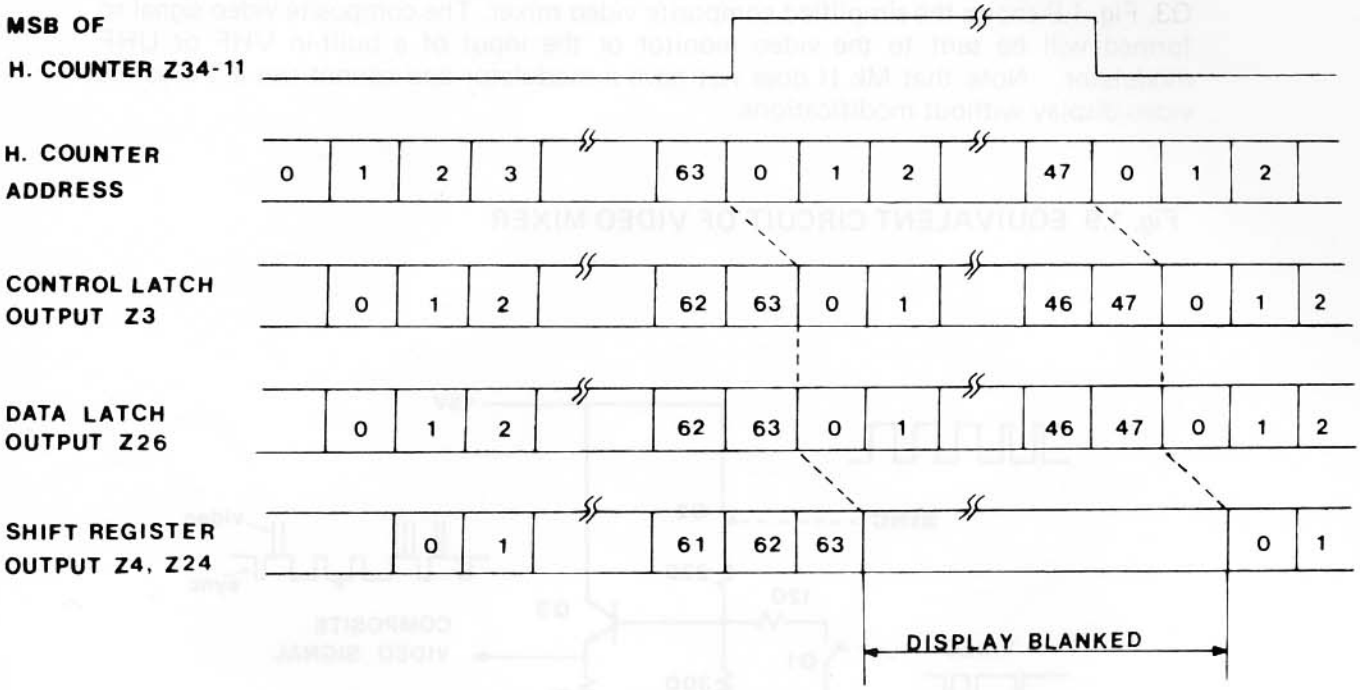


Fig. 1.8(b) VIDEO DISPLAY TIMING OF A LINE



NOTE: The numbers in the control and data latch timings represent the control or data signals of the corresponding horizontal address.

In the graphic mode, each row contains 64 graphic units in 12 scanning lines, and each unit is made up by 6 cells. Each cell corresponds to one data bit in the RAM. Details refer to section 1.4.4.2 on graphic data.

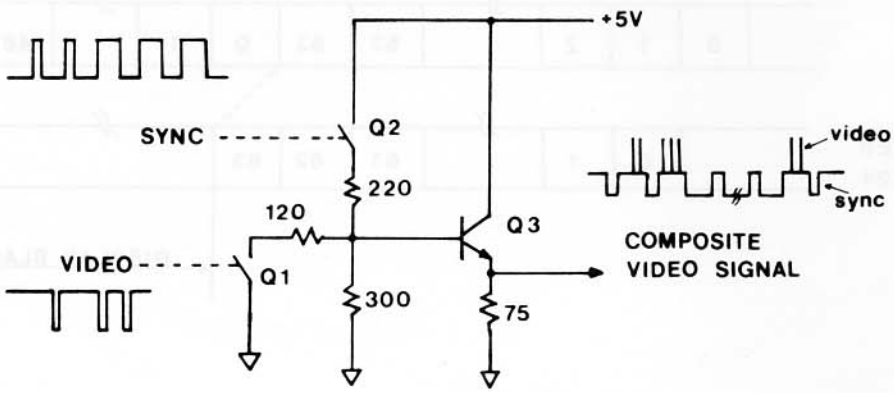
The generation of video signals in the graphic mode is similar to that in the character mode. They differ in that a multiplexer, Z27 and shift register, Z4 are used in the graphic mode. Since D7 of a graphic data is one, and then Z3-7 is HIGH, Z4 will be enabled to accept the graphic data from Z27. The dot signals will be shifted out serially at Z4-13 at the rate of 10.644 MHz. Note that the multiplexer, Z27 is controlled by L3 and L2, and the graphic data from the latch, Z26 are fed to Z27 instead of the character generator, Z25.

Display blanking is achieved as follows. Scanning lines 9-11 in the character mode are automatically blanked because the outputs of the character generator will be zero during these 3 lines. The horizontal and vertical blanking signal comes from Z11-1 and inhibits Z24 and Z4 from getting parallel data from Z25 and Z27 respectively. The display is blanked during the period of screen boundary and retrace when the horizontal or vertical sync signal is HIGH at pin 2 or 3 of Z11 respectively. See Fig. 1.8(b).

1.4.3 Composite Video Signal

The horizontal sync and the vertical sync signals are combined by Z22, and this composite sync signal is fed to the base of Q2. Q1 and Q2 act as two switches. Q3 forms a mixing circuit, and the sync and video signals are summed up at the base of Q3. Fig. 1.9 shows the simplified composite video mixer. The composite video signal so formed will be sent to the video monitor or the input of a built-in VHF or UHF modulator. Note that Mk II does not have a modulator and cannot use a TV as the video display without modifications.

Fig. 1.9 EQUIVALENT CIRCUIT OF VIDEO MIXER



1.4.4 Display Modes

The System-80 has two display modes, namely, character mode and graphic mode. Data bit 7 of the video memory determines the mode of display; character mode is selected when D7 is logical '0' and graphic mode when D7 is logical '1'.

1.4.4.1 Character Mode

The characters displayed are in alphanumeric format, and their ASCII codes are stored in the video RAM's. In the preceding sections, 64 characters/line mode is assumed. The MKI System-80 has a push-button, S1 at the back panel of the unit to select either 64 characters/line or 32 characters/line mode. The MKII System has no 32 characters/line mode of display.

In 32 characters/line mode, switch S1 is closed. Multiplexers Z29 and Z37 are switched to the other four inputs. The reference counter clock becomes CLOCK/2 so that the horizontal/vertical counting frequencies will be scaled down by two. The PAGE switch chooses the left page when LOW, and chooses the right page when HIGH. This is obvious because A5 of the video RAM is connected to the PAGE signal through the multiplexer Z37, and address bits A0 – A5 select one of the 64 columns in the 64 x 16 units of bytes of video memory.

1.4.4.2 Graphic Mode

D7 is logical one when graphics are to be displayed. The shift register Z4 is enabled. The graphic data from the video RAM are latched into Z26, and the outputs of Z26 are multiplexed by Z27 (74LS153) selecting two out of six bits each time. The selection is controlled by the line count signals, L2 and L3. A graphic cell is specified as below.

1 graphic unit

(6 graphic cells)

DØ	D1
D2	D3
D4	D5

D0 and D1are selected for scan lines 00 – 03, D2 and D3 for scan lines 04 – 07, D4 and D5 for scan lines 08 – 011.

The display formats of the character/graphic modes are shown in Fig. 1-10.

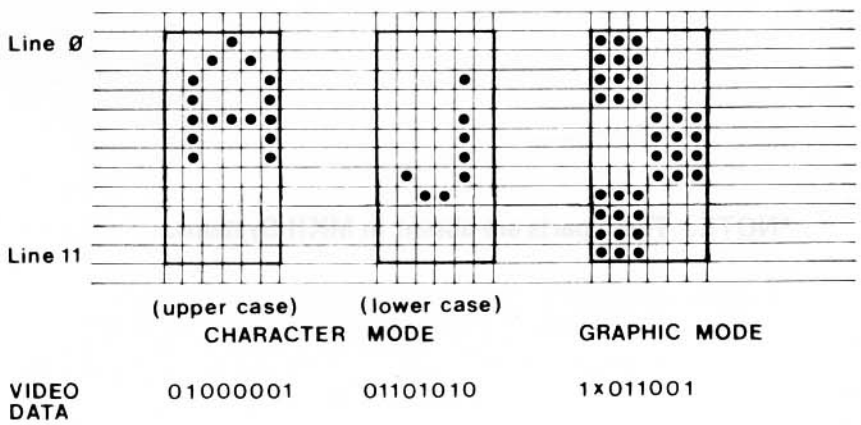
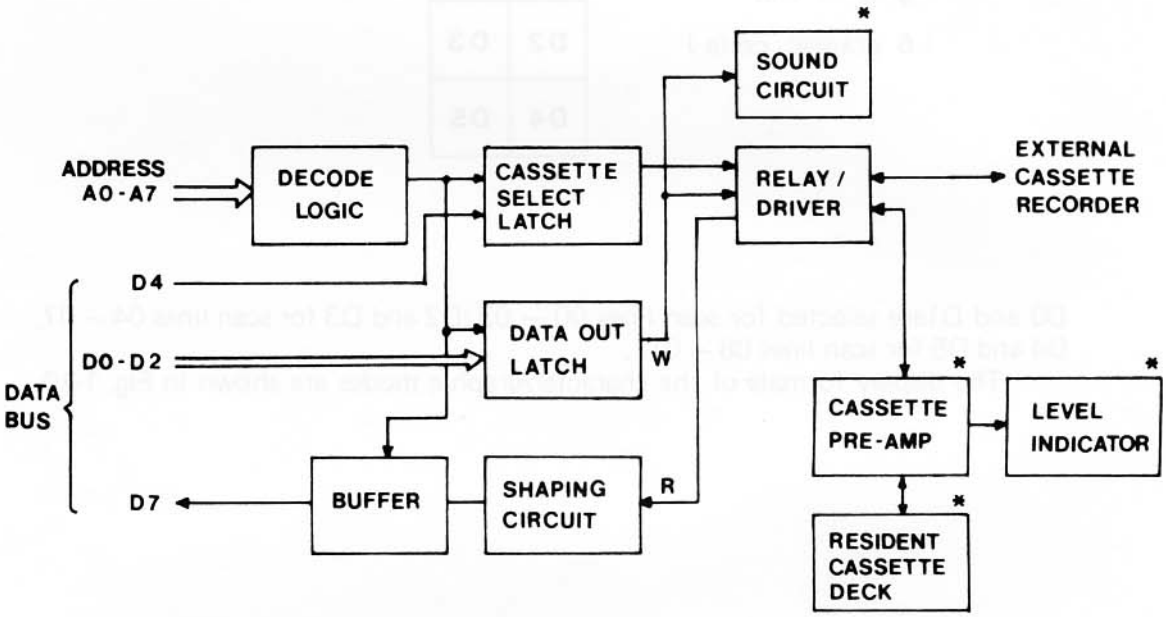


Fig. 1-10 CHARACTER/GRAPHIC DISPLAY FORMAT

1.5 CASSETTE INTERFACE

The cassette interface consists of the following parts: address decoding, latches, cassette select and relay drivers, rectifying and shaping circuit, and cassette preamplifiers and output level indicator. See Fig. 1.11. Sound effect circuit also uses the cassette output port.

Fig. 1.11 CASSETTE INTERFACE



*NOTE: These parts are absent in MKII Systems.

1.5.1 Addressing/Decode

Z19, Z31 and Z20 generate the address decode signals and the I/O control signals. Table 1.1 shows the I/O port assignments.

Table 1.1 CASSETTE I/O PORT

PORT	DATA BITS			HIGH	LOW
Output, FF	D2			Cassette ON	Cassette OFF
	D0, D1	signal	output		
Input, FF	D7	signal	input		
Output, FE	D4			Cassette 2 Selected (external)	Cassette 1 Selected

1.5.2 Cassette Selection

The CPU selects either cassette 1 or cassette 2 through the output port FE with data line, D4. The selecting signal from D4 is latched by Z40, and outputs at Z40-8 ($\overline{Q}$) and Z40-9 (Q). cassette 1 is selected as D4 is LOW, and Q7 and Q8 will turn ON provided D2 (at Z6-2) is HIGH. Relay REL1 will be activated, and the READ, WRITE and motor drive lines of the resident cassette 1 will be connected to the cassette interface.

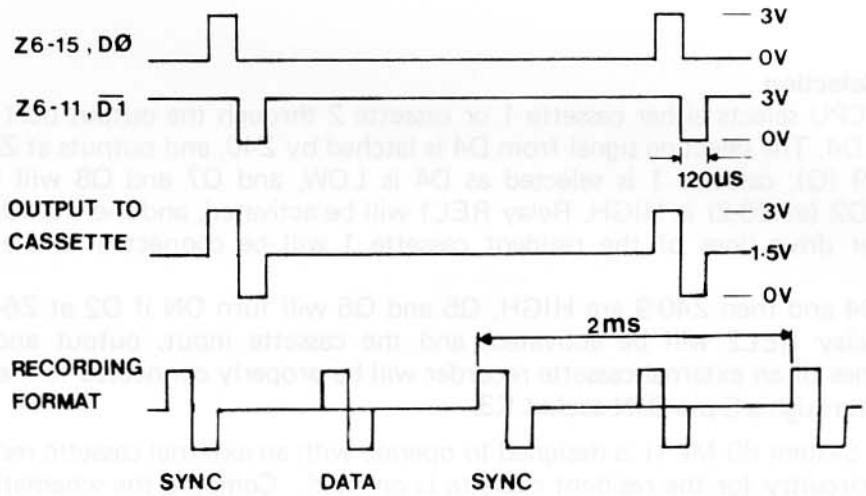
As D4 and then Z40-9 are HIGH, Q5 and Q6 will turn ON if D2 at Z6-2 is also HIGH. Relay REL2 will be activated, and the cassette input, output and remote control lines of an external cassette recorder will be properly connected to the cassette interface through a 5-pin DIN socket K3.

The System 80 Mk II is designed to operate with an external cassette recorder, so that the circuitry for the resident cassette is omitted. Compare the schematics of the cassette interfaces for the System 80 Mk I and Mk II.

1.5.3 Cassette Write

The idealized recording signal to be stored on the cassette tape is shown in Fig. 1.12. This signal is formed by data D1, D0 and a summing circuit at Z6-11 ($\overline{Q}$) and Z6-15 (Q). The logical outputs of D1 and D0 are software controlled to construct the desired recording signals.

Fig. 1.12 CASSETTE WRITE SIGNALS

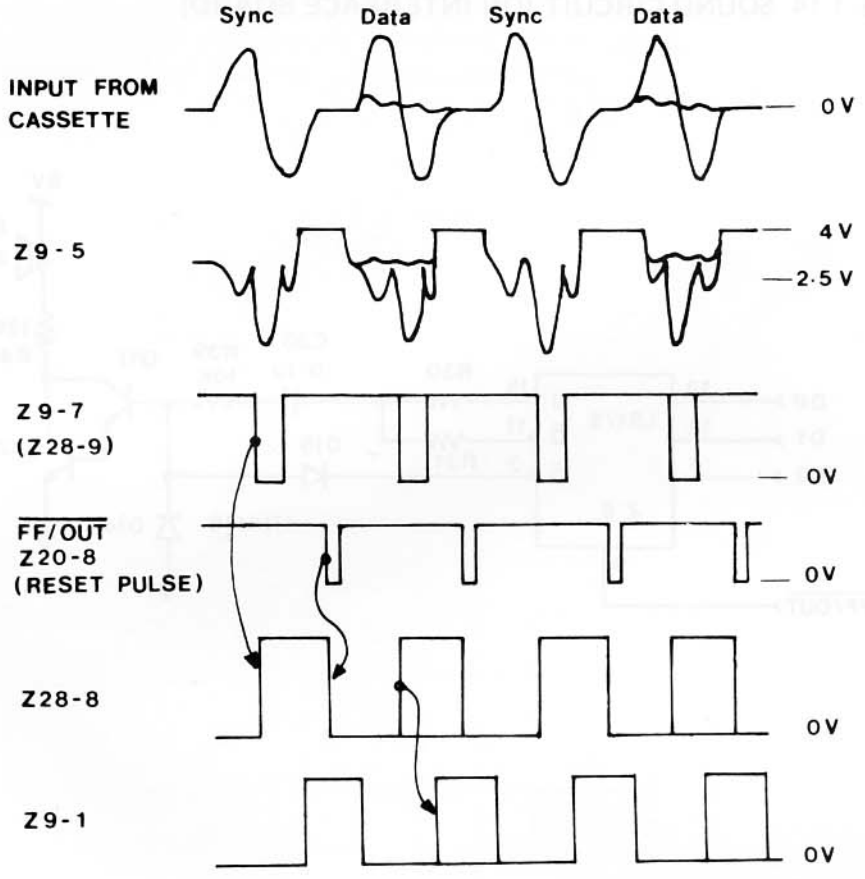


The data format stored on the cassette tape is as follows. At the beginning of cassette write (CSAVE), the CPU outputs 128 ZERO data bits, followed by a code A5H. The CPU will detect this code during cassette read (CLOAD) for synchronization. Next come a two-byte starting address and a two-byte ending address of the program in the RAM's. After all data have been written, a byte of check-sum is added for detecting errors during cassette read/write.

1.5.4 Cassette Read

Before the CPU can recognise the information retrieved from a cassette tape, the audio signal from the cassette recorder must be shaped into logical sync and data signals. The CPU and cassette routine will then convert the serial data into source programs which will be stored into the RAM's. The filtering pre-amplifiers formed by Z1 (LM324) on the cassette board amplify the small signals from the Read/write head. The amplified signal is buffered (Q1) and rectified to drive a level meter. This signal level indication is useful in cassette reading various tapes. We may obtain the proper signal level by adjusting the gain of Z1 (VR3).

Fig. 1.13 CASSETTE READ SIGNALS

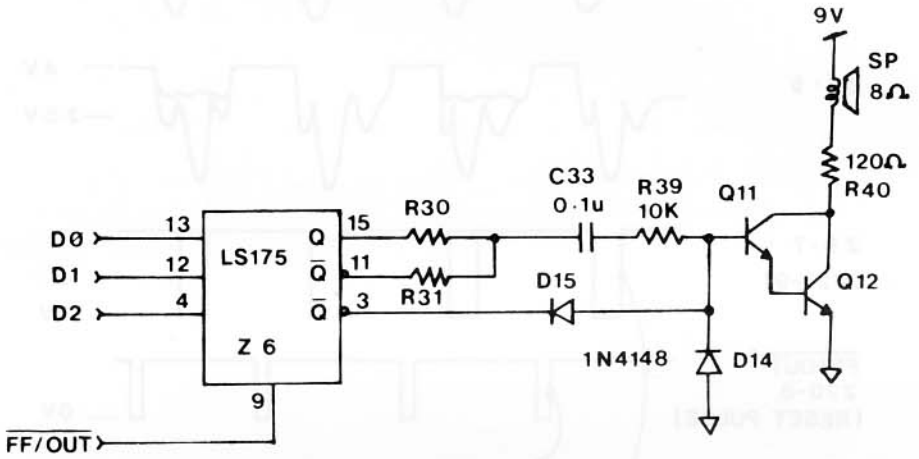


Z9 (LM324) on the interface board converts the audio signal from the recorder into serial digital signal. The input signal is high-pass filtered, and then full-wave rectified. Negative-going pulses are obtained at Z9-7, the output of a level detector. Z9-7 is connected to Z28-9. Z28 forms a R-S bistable latch, and Z28-8 is connected to the data line, D7 through a buffer, Z7. Z28-8 is triggered to HIGH by the falling edge at Z9-7. As soon as the CPU has read a logical 1 at data line D7, it will reset the bistable latch after 500 usec. Upon detecting the leading zeroes and the sync code (A5H), the CPU should be synchronized with the serial data stream. It will strobe the data pulse at 1 msec after the sync pulse and reset the bistable latch. Pulses at Z28-8 are delayed for about 250 usec and output at Z9-1. The delayed pulse pulls up the signal at Z9-5, and therefore, the signal-to-noise ratio is increased.

1.5.5 Sound Output (Blue Label Machines only)

Apart from video display, sound effects are another way of communication between a man and the System-80 microcomputer. This is implemented simply by an audio driver (Q11 and Q12 darlington) and a built-in loudspeaker. The sound circuit is connected to the cassette output port FFH. The sound output is determined by the software outputting various data stream to D0 and D1 of the output port. See Fig. 1.14. The sound stops during CSAVE because the base of Q11 is pulled LOW by Z6-3 ($\bar{Q}$ of D2). D2 of the output port FFH becomes HIGH during cassette ON.

Fig. 1.14 SOUND CIRCUIT (ON INTERFACE BOARD)



1.6 KEYBOARD

The key matrix is memory mapped with addresses from 3800H to 3880H, and locations 3800H – 3BFFH are reserved for keyboard use. Refer to the memory map in Fig. 1.2.

There are two locked switches, F1 and PAGE which are not included in the key matrix. They directly control the hardware of the resident cassette recorder and the display modes respectively. These two keys are absent in MKII machines which have no resident cassette recorder.

1.6.1 Key Matrix

The key matrix is formed by 8 inverted address lines AK0 – AK7 and 8 inverted data lines DK0 – DK7. The matrix is illustrated in Fig. 1.15.

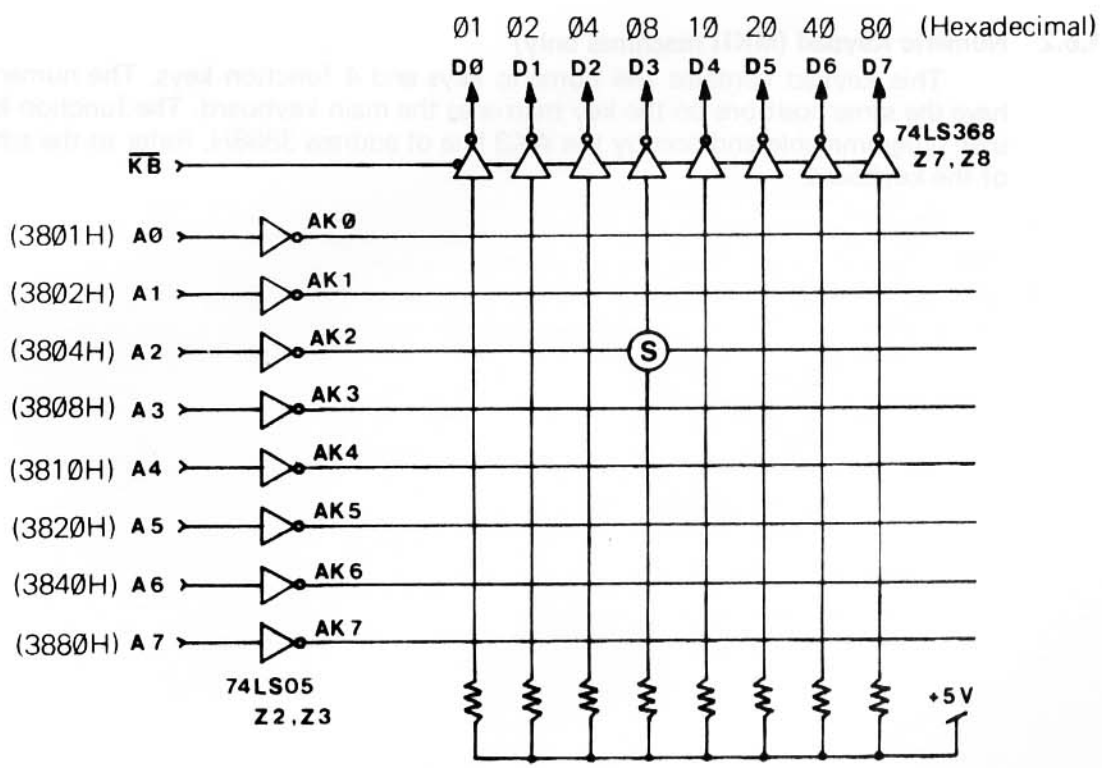


Fig. 1.15 KEY MATRIX

The inverting buffers, Z7 and Z8 are controlled by the keyboard strobe, $\overline{KB}$ which is derived from Z35 – 11 on the CPU board. Refer to section 1.1.4. $\overline{KB}$ is active LOW when the CPU is accessing the memory locations 3800H – 3BFFH. AKØ – AK7 are the open-collector outputs of Z2 and Z3 (74LS05).

While no key is pressed, DKØ – DK7 are all HIGH since they are pulled up to +5V by resistors. The CPU reads ØØH, indicating no key is pressed. The keyboard routine in the system ROM scans through the AØ – A7 lines repeatedly, making one address line logic HIGH each time. See Fig. 1.15. When any key is depressed, the CPU will detect a logic HIGH on the corresponding data line as soon as the corresponding address line is scanned. For instance, key S is depressed. The DK3 line will be connected to the AK2 line, and DK3 will be LOW as A2 is logic HIGH. Then, the CPU will read Ø8H into the accumulator from the memory location 3804H. The keyboard routine will decode it into the ASCII equivalent of the character S. Except the command keys, the ASCII codes of the characters or symbols keyed in will be written into the video RAM and displayed.

1.6.2 Numeric Keypad (MKII machines only)

This keypad contains the numeric keys and 4 function keys. The numeric keys have the same positions on the key matrix as the main keyboard. The function keys are user programmable and occupy the AK3 line of address 3808H. Refer to the schematic of the keyboard.

1.7 POWER SUPPLY

The power supply unit which is in a heat-resisting plastic box delivers full-wave rectified +8VDC, +16VDC and −16VDC. The two power transformers have secondary voltages of 9.6V x 2 and 15V x 2 respectively. At the primary side of the transformers, there is a line filter network composed of a parallel ceramic capacitor of 0.01uF and two series RF chokces. Overvoltage protection is provided by a varistor across the ac mains. The metal oxide varistor has a breakdown voltage of 275V with 55 joules. Over-load and short-circuit damages are minimized by a fuse of 0.5A in series with the ac mains.

The specifications for the output voltages of the power supply unit are as below.

Voltage	No load voltage		Full load voltage		Remark
	Min.	max.	min.	max.	
+8V	10.5V	11.5V	8V	9V	FL +8V @ 1.2A
+16V	20V	24V	15V	18V	FL +16V @150mA
−16V	20V	24V	15V	18V	FL −16V @ 100mA

Linear IC regulators 7805 and 7812 on the CPU board supply +5V and +12V respectively. A simple zener regulator provides −5V for the dynamic RAM's. On the interface board, +9V supply is obtained from +16V by a transistor/zener regulating circuit (Q10 and 10V zener diode). +9VDC is required for driving the relays on the interface board, the pre-amplifier (Z1, LM324) on the cassette board, and the motor of the resident cassette recorder.

1.8 RS-232-C Interface

The X-4022 RS-232-C Interface gives you the flexibility of:

i) a wide range of useful baud rate: 110, 300, 600, 1200, 2400, 4800, 9600, and 19200
ii) selectable word length; 5, 6, 7 or 8 bits
iii) selectable 1 or 2 stop bits
iv) optional parity bit, and selectable even or odd parity.

On the RS-232-C Interface card, there are two dip-switches. The one along the middle row is called DP1 (with red paint marking), and the other is called DP2.

If you wish to use the RS-232-C Interface to operate serial printers, set switches 6, 7 and 8 of DP1 to OFF, ON and OFF respectively. Then, you can use the LPRINT and LLIST commands for your hard copy print out from a serial printer. While the serial printer interface is in use, the parallel printer interface will be disabled automatically.

Otherwise, switches 6, 7 and 8 of DP1 should be set to ON, OFF and ON positions respectively for normal communication operation. And, the parallel printer function is recovered.

FUNCTION	DP1		
	S6	S7	S8
SERIAL PRINTER (WO handshaking)	OFF	ON	OFF
SERIAL PRINTER (with handshaking)	ON	ON	OFF
COMMUNICATION	ON	OFF	ON

Flip switches 1 to 5 of DP1 to select the desired functions that are suitable for your RS-232-C device.

DP1	FUNCTION	
	ON	OFF
S1	PARITY ENABLED	PARITY INHIBITED
S2	1 STOP BIT	2 STOP BITS*
S5	ODD PARITY	EVEN PARITY

*Note: If 5 bits/character is selected, this will produce 1½ stop bit.

Switch 4 and 3 of DP1 select number of bits per character.

NO. OF BITS PER CHARACTER	DP1	
	S3	S4
5	ON	ON
6	ON	OFF
7	OFF	ON
8	OFF	OFF

Select the desired baud rate by flipping switches of DP2 in proper positions as below:

BAUD RATE	DP2							
	S1	S2	S3	S4	S5	S6	S7	S8
19200	ON	—	—	—	—	—	—	—
9600	—	ON	—	—	—	—	—	—
4800	—	—	ON	—	—	—	—	—
2400	—	—	—	ON	—	—	—	—
1200	—	—	—	—	ON	—	—	—
600	—	—	—	—	—	ON	—	—
300	—	—	—	—	—	—	ON	—
110	—	—	—	—	—	—	—	ON

NOTE: — means in OFF position

The address decode scheme is as follows:

PORT FUNCTION	ADDRESS (HEX)	INPUT TO CPU	OUTPUT TO INTERFACE
SERIAL INPUT PORT	F8	DATA	STATUS
SERIAL OUTPUT PORT	F9	STATUS	DATA
SERIAL PRINTER	FD	STATUS	DATA

Bit Assignment for Status Ports:

DATA BIT	COMMUNICATION OUT PORT F8H	COMMUNICATION IN PORT F9H	SERIAL PRINTER IN PORT FDH
DØ	Request to send DB-25 Pin 4	Data available 1 = true	unused
D1	Data Terminal Ready DB-25 Pin-20	Overrun error 1 = true	unused
D2	UART reset 1 = true	Framing error 1 = true	unused
D3	unused	Parity error 1 = true	unused
D4	unused	Carrier Detect DB-25 Pin 8	Carrier Detect DB-25 Pin 8
D5	unused	Data Set Ready DB-25 Pin 6	Data Set Ready DB-25 Pin 6
D6	unused	Clear to send DB-25 Pin 5	Always Low
D7	unused	Transmitting Buffer Empty 0 = true	Transmitting Buffer Empty 0 = true

The pin assignment for RS-232-C Interface:

PIN	SIGNAL	DESCRIPTION	
1	PGND	Protective Ground	
2	TXD	Transmit Data	(OUT)
3	RXD	Receive Data	(IN)
4	RTS	Request-to-send	(OUT)
5	CTS	Clear-to-send	(IN)
6	DSR	Data Set Ready	(IN)
7	SGND	Signal Ground	
8	CD	Carrier Detect	(IN)
20	DTR	Data Terminal Ready	(OUT)

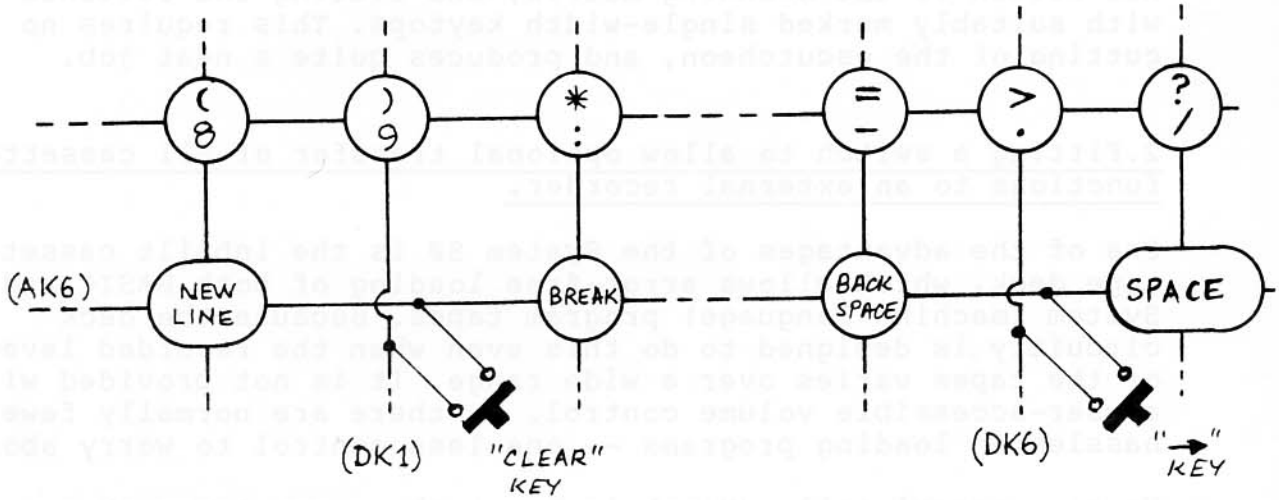
1.9 MINOR MODIFICATIONS TO EARLIER SYSTEM-80 COMPUTERS

1.Providing "forward arrow" and "CLEAR" keys.

The keyboard of earlier System-80 computers does not provide the "forward arrow" (→) or "CLEAR" keys as provided on the keyboard of the Tandy TRS-80 machine. This is generally not a major problem, as neither key is frequently used. However there are some existing TRS-80 programs where one or other is used.

Where such programs are written in BASIC, it is usually a fairly simple matter to modify the program so that it uses other keys. But this is generally not as easy to do with machine language or "System" programs.

As it happens, the addition of extra keys on the System 80 keyboard to provide the extra functions is electrically very simple. The keyswitches are arranged in a matrix which is software scanned, and the matrix positions which in the TRS-80 are occupied by both keys are currently vacant. So all that is needed are two additional pushbuttons or keyswitches, and four lengths of wire to connect them thus:



As you can see, the "forward arrow" key connects to the DK6 and AK6 scanning lines of the keyboard PCB, while the "CLEAR" key connects to the DK1 and AK6 lines.

But while this modification is electrically simple, it is not so easy mechanically. Ideally, perhaps, the switches would be mounted immediately to the right of the "BACKSPACE" key; but this would require cutting mounting holes in both the keyboard escutcheon and the metal mounting plate. The latter would mean removal of all the keyswitches, and few would be prepared to do this.

The exact approach used is a matter for the individual owner. Low-cost pushbuttons (like DSE Cat. No.S-1102) could be used, and mounted in holes drilled in the panel escutcheon at convenient places.

Another possibility, and a rather neater one, is to fit the new keyswitches in place of the right-hand SHIFT key. This requires removal of the present double-width keytop, replacement of the present dummy spring unit alongside the shift keyswitch with a second switch, rewiring the existing switch and wiring of the new switch to the scanning matrix, and fitting the switches with suitably marked single-width keytops. This requires no cutting of the escutcheon, and produces quite a neat job.

2.Fitting a switch to allow optional transfer of all cassette functions to an external recorder.

One of the advantages of the System 80 is the inbuilt cassette tape deck, which allows error-free loading of both BASIC and System (machine language) program tapes. Because the deck circuitry is designed to do this even when the recorded level of the tapes varies over a wide range, it is not provided with a user-accessible volume control. So there are normally fewer hassles in loading programs -- one less control to worry about!

However occasionally (Murphy's Law!) there are tapes whose recorded level is either too high or too low to load correctly with the internal deck's preset circuit.

With BASIC tapes there is no problem, because the CLOAD#-2 command can be used to load them via an external recorder with adjustable volume control. But this cannot normally be done with System tapes, as the SYSTEM command only loads tapes via the internal tape deck ("cassette No.1").

A similar problem occurs if you want to connect up to your System 80 a low-cost light pen designed for use with the TRS-80 (such as the X-3645). Such pens are designed to use the cassette recorder as a preamplifier; they plug into the recorder's MIC input. However there is no MIC input provided for the System 80's inbuilt cassette deck.

The answer is to use an external recorder, and plug the light pen into it. However the software normally supplied with the light pens is designed for a standard TRS-80, and accordingly it expects the pen to be connected to "cassette No.1". Although the software can be modified, this can be tedious and time-consuming especially with machine-language programs.

A neater way of overcoming both of the above problems is to fit a simple switch to allow the internal cassette deck to be optionally disabled, and its functions transferred entirely to an external recorder. This effectively converts the System 80 cassette circuit into an exact replica of that in the TRS-80.

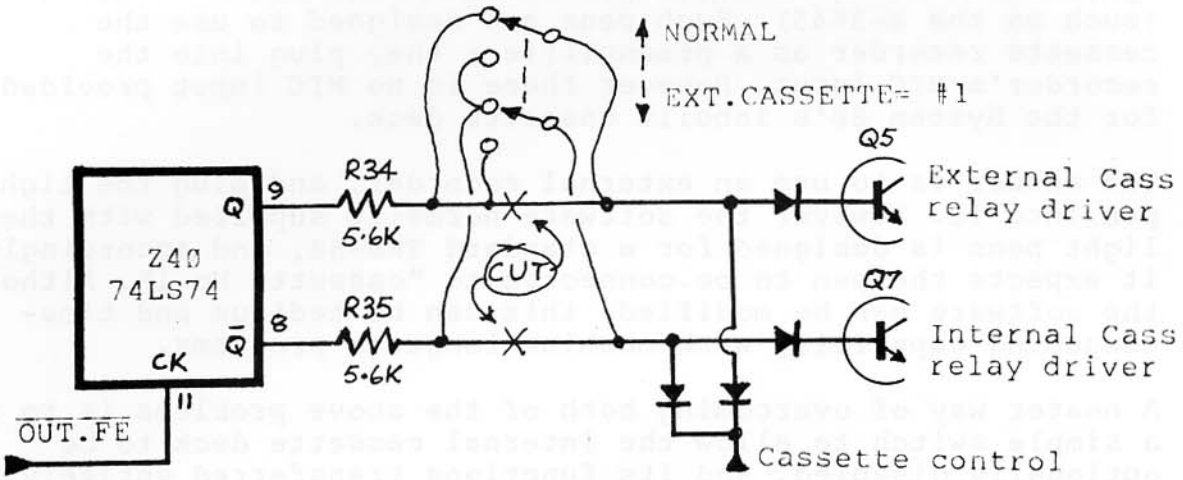
Basically, the System 80's cassette I/O circuit is exactly like that of the TRS-80 in that all data and control is transferred via I/O port address FF hex (255 decimal). However because the System 80 has provision for two cassette recorders, additional circuitry has been added to allow connection of either one cassette or the other to the I/O circuitry.

The additional circuitry consists of a latch flipflop provided with decoding so that it effectively resides at a second I/O address FE hex (or 254 decimal). Each cassette recorder circuit is controlled by a small relay, and the relay driver circuits are enabled by the two outputs (Q and Q-bar) of the latch flipflop. If hex 10 (decimal 16) is fed to I/O port FE, the latch flipflop is set, enabling the "cassette No.2" relay driver and allowing the external recorder to respond to normal tape communication via port FF. At the same time the "cassette No.1" relay driver is disabled, preventing that recorder from responding.

Conversely if hex 00 (decimal 0) is fed to I/O port FE, the latch flipflop is reset, disabling the "cassette No.2" driver and enabling that for cassette No.1". This is the normal circuit condition, with the internal cassette deck enabled.

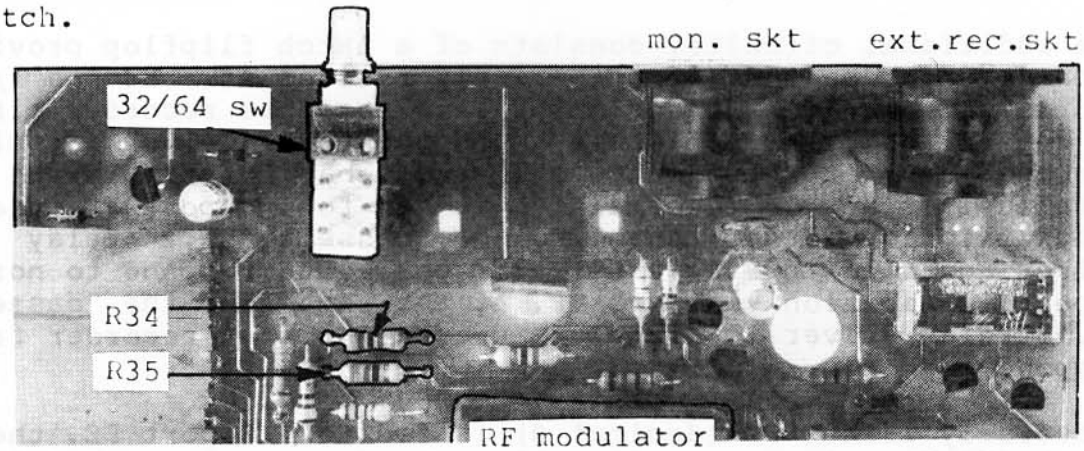
To enable the external recorder to be used instead of the internal deck, without software changes, all that is required is the addition of a DPDT switch to allow optional disabling of the "cassette No.1" relay driver, and connection of the other driver to the Q-bar latch output instead of the Q output. This makes the external recorder <u>become</u> "cassette No.1" as far as the software is concerned.

In schematic form the change looks like:



Mechanically the mod is easiest done by lifting one end of the series resistors R34 and R35 from the PCB. Four wires can then be run to a small slider, toggle or pushbutton switch.

R34 and R35 are easy to find: they are on the top of the System 80's interface PCB, at the rear and just to the front of the pushbutton switch for 32/64 character line selection. The resistor for the external cassette drive, R34, is nearest the switch.



Probably the easiest place to fit the extra switch is on the lower back of the case, below the space between the 32/64 character button and the video output socket. Quite short wires can then be used to connect it to the resistors and PCB.

Don't forget the link between the switch contacts!

3. Note about length of System 80 BASIC statement lines:

As with the TRS-80, BASIC statement lines for the System 80 may be up to 255 characters long (total length including the line number). However in exactly the same fashion as the TRS-80, the System 80 will only allow you to key in up to 240 characters in the normal entry mode. This is normally far more than is needed. However if you really must have a line of the full 255 characters, you have to go to EDIT mode and use the "X" command to add the remaining 15 characters.

4. Note about System 80 keytop legends:

The following points should be noted about the legends used on the System 80 keytops:

(a) The NEW LINE key is functionally identical to the ENTER key on a TRS-80.

(b) The BACKSPACE key is identical to the "back arrow" (←) key on a TRS-80.

(c) The CTRL key is identical to the "down arrow" (↓) key.

(d) The ESC key is identical to the "up arrow" (↑) key.

(e) Although the "at sign" (@) key shows a "backslash" sign as its shift mode character, this character is not available. Pressing the key with the shift key held down still gives the @ character. This is exactly the same as the TRS-80.

5. Note about the VAL string function:

If the BASIC string function VAL is used with an argument in which the number part of the string is followed by a percent sign (%), the System 80's Level II interpreter will throw out the statement with a ?SN ERROR. This is also exactly the same as the TRS-80. The remedy is not to use a percent sign!

DIFFERENCES BETWEEN THE SYSTEM-80 AND TRS-80 COMPUTERS

AFFECTING SOFTWARE COMPATIBILITY

There are a number of small hardware differences between the Dick Smith System-80 computer and the Tandy TRS-80 Model 1, Level II computer which affect software compatibility to some extent. These are described below.

It is important to realise, however, that in general the hardware differences do not affect programs written in BASIC language, because in each machine the BASIC interpreter program built into the machine's ROMs is designed to suit the machine's hardware. Many machine language programs also are unaffected, either because the differences are not relevant or because the programs "call" driver routines in the BASIC ROMs to communicate with the hardware. The only programs which are affected are those which use their own driver routines, and the routines are designed to communicate specifically with the hardware of one machine.

1. CASSETTE INTERFACE

The System-80 has a cassette deck built into the basic machine, as well as a socket for a second external recorder. It has circuitry inbuilt to allow software selection of recorders, whereas with the TRS-80 selection circuitry is provided only in the Expansion Interface. Because of this, programs which use the cassette port (either for communication with a cassette, or for operation of a light pen, sound effects unit,etc), if they are written for the TRS-80, may not run properly on a System-80 without modification.

The cassette interface on both machines uses I/O address "FF" hex as its data port, with bits B0 and B1 for the data itself. However the machines differ slightly in their use of bit B2: in the TRS-80 this is used solely for cassette motor control, whereas in the System-80 it is also used to enable data paths to both recorders. Unless this bit is set high (B2=1) in a System-80, no output data can pass from the computer to the external recorder socket, and no input data can pass from the internal deck to the computer. Note that this bit must be set high each time output data is fed to port FF.

The two machines also differ in the address used to perform software switching between the two recorders. In the System-80, the switching is done by a latch at I/O address "FE" hex, and specifically by bit B4 at that address. The corresponding latch in the TRS-80 Expansion Interface is at memory address "37E4" hex, and responds to bit B0. In both cases setting the bit low corresponds to cassette #1, and setting it high corresponds to cassette #2.

2. PRINTER INTERFACE

Both machines allow for a printer. However the printer port in the System-80 uses I/O address "FD", whereas that in the TRS-80 uses memory address "37E8". This does not affect the BASIC command LLIST, or the statement LPRINT, or machine language programs which utilise the BASIC interpreter's printer routine (like Microsoft's Editor/Assembler-Plus). But it does affect programs having their own printer driver, like the Tandy Editor/Assembler and Word Processor.

Note, however, that the System-80 Expansion unit gives the user a choice of placing either the Centronics-type parallel port or the RS-232C serial port at the printer address "FD". This allows the use of a teleprinter in place of a parallel printer.

3. SERIAL INTERFACE

The two machines differ here again in terms of the ports used for data and UART/terminal status interfacing. In the System-80, I/O addresses "F8" and "F9" are used, whereas the TRS-80 uses memory addresses "37DE" and "37DF".

With the System-80, output data to the UART is written to port F9, while input data from the UART is read from port F8. Conversely output status/control information is written to port F8, while input status information is read from port F9. In the TRS-80, address 37DF is used for both input and output of data, while address 37DE is used for input and output of status information.

4. KEYBOARD DIFFERENCES

Early models of the System-80 as supplied do not provide two keys present on the TRS-80 : the "Right Arrow" and "CLEAR" keys. This obviously affects software which uses these keys, calling for either changes to the programs or addition of one or both keys.

5. VIDEO DISPLAY OF "ARROW" KEYS

As explained overleaf there is a difference between the two machines in the video display of ASCII codes 91,92,93 and 94 (decimal). The System-80 displays the normal ASCII characters corresponding to these codes ("[","\","^" and "]", whereas many (but not all) TRS-80 machines display four "arrow" symbols ("↑","↓","→" and "←") to match their arrow keys. However note that some early TRS-80s do display the square opening bracket "[" for code 91, instead of the upward arrow.

SYSTEM 80 VIDEO DISPLAY CODES.

1. GRAPHICS CODES 128-191 (8Ø-BF hex):

There is no difference between the System 80 and the TRS-80 Level II in terms of the graphics characters displayed on the video screen for ASCII Codes 128-191 inclusive. To emphasise this and for reference, a full listing of these graphics characters is attached.

2. SPACE COMPRESSION CODES 192-255 (CØ-FF hex):

As with the TRS-80, the System 80 uses the codes 192-255 for space compression or horizontal tabulation. So in both cases, these codes give from Ø to 63 spaces: 192 gives no space, 193 gives 1 space, 194 gives 2 spaces and so on, up to code 255 which gives 63 spaces.

BUT NOTE that these codes have this effect only when used in a PRINTCHR$(N) statement or command. When used in a direct POKE A, N statement to screen RAM, the codes simply duplicate the graphics codes 128-191. I.e., code 192 gives the same graphics character as 128, 193 the same as 129, and so on.

3. ALPHANUMERIC CODES 32-127 (2Ø-7F hex):

For codes 32-90 inclusive and code 95, the System 80 gives exactly the same alphanumeric character set as the TRS-80 machine. A listing is attached. However for codes 91, 92, 93 and 94, the System 80 follows standard ASCII code rather than display the special "arrow" characters displayed by the TRS-80 (although some TRS-80s also display the standard "Square opening bracket" character for code 91).

Codes 96-127 are used for producing the normal lower-case alphabetic characters with a printer. However it should be noted that if these codes are fed to the video display, the lower case characters are not generated. The characters which are displayed will depend again upon whether you use a PRINTCHR$(N) or a POKE A,N statement.

If your machine is not fitted with lower case software and hardware and you use a PRINT CHR$(N) statement or command, the codes will duplicate the upper-case alpha codes 64-95. But if you use a POKE A,N statement or command, the codes will generate the punctuation and numeric codes 32-63 as shown in the third attached listing.

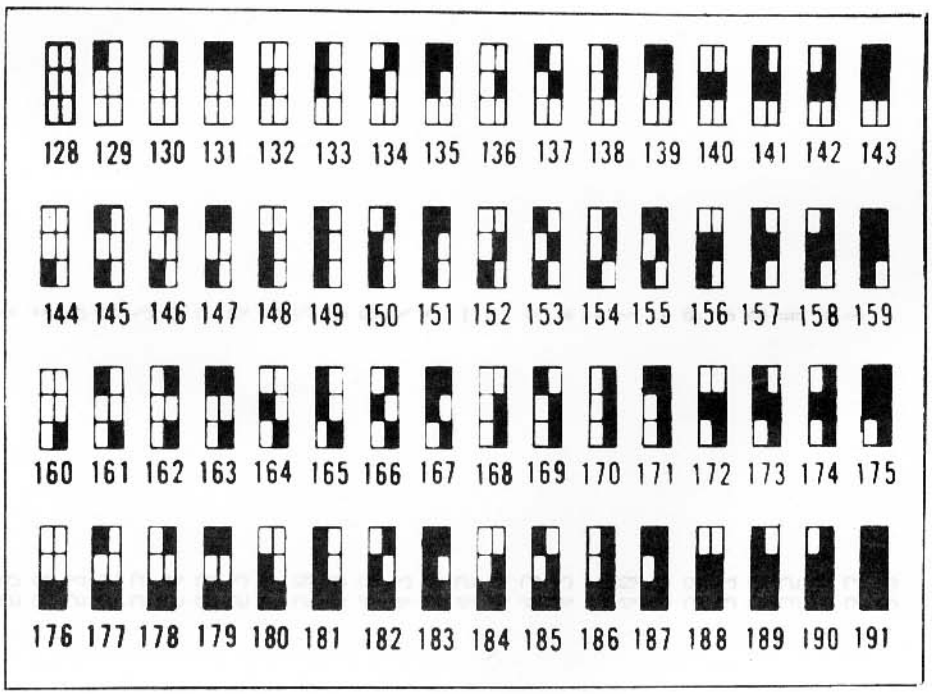
So these codes may be used flexibly, now you know what the results will be.

4. CONTROL CODES Ø-31 (ØØ-1F hex):

As explained in the System 80 BASIC Manual, these produce exactly the same results as for the TRS-80. Note, however, that codes 10-13 inclusive all produce a carriage return--line feed combination on the video screen (even though codes 11 and 12 control TOF functions with a printer).

NOTE ALSO that the System 80's "32 character/line" mode, as produced by a PRINTCHR$(23) statement, is not identical with that on a TRS-80. In the System 80 this mode simply causes any new characters added to the screen RAM to be separated by single spaces. They remain of normal width, not double width as with the TRS-80. Reversion to normal 64 characters/line mode will occur upon resetting, execution of a CLS command or statement, or execution of a PRINTCHR$(28) command or statement.

SYSTEM 8Ø COMPUTER -- ASCII CODES 128-191



SYSTEM 80 COMPUTER -- ASCII CODES 32-127 AS DISPLAYED ON VIDEO SCREEN:

CODE	CHARACTER	CODE	CHARACTER	CODE	CHARACTER
32		64	@	96	
33	!	65	A	97	!
34	"	66	B	98	"
35	#	67	C	99	#
36	$	68	D	100	$
37	%	69	E	101	%
38	&	70	F	102	&
39	'	71	G	103	'
40	(	72	H	104	(
41	)	73	I	105	)
42	*	74	J	106	*
43	+	75	K	107	+
44	,	76	L	108	,
45	-	77	M	109	-
46	.	78	N	110	.
47	/	79	O	111	/
48	0	80	P	112	0
49	1	81	Q	113	1
50	2	82	R	114	2
51	3	83	S	115	3
52	4	84	T	116	4
53	5	85	U	117	5
54	6	86	V	118	6
55	7	87	W	119	7
56	8	88	X	120	8
57	9	89	Y	121	9
58	:	90	Z	122	:
59	;	91	[	123	;
60	<	92	\	124	<
61	=	93	]	125	=
62	>	94	^	126	>
63	?	95	_	127	?

SYSTEM 80 COMPUTER -- ASCII CODES 32-127 AS PRINTED:

CODE	CHARACTER	CODE	CHARACTER	CODE	CHARACTER
32		64	@	96	`
33	!	65	A	97	a
34	"	66	B	98	b
35	#	67	C	99	c
36	$	68	D	100	d
37	%	69	E	101	e
38	&	70	F	102	f
39	'	71	G	103	g
40	(	72	H	104	h
41	)	73	I	105	i
42	*	74	J	106	j
43	+	75	K	107	k
44	,	76	L	108	l
45	-	77	M	109	m
46	.	78	N	110	n
47	/	79	O	111	o
48	0	80	P	112	p
49	1	81	Q	113	q
50	2	82	R	114	r
51	3	83	S	115	s
52	4	84	T	116	t
53	5	85	U	117	u
54	6	86	V	118	v
55	7	87	W	119	w
56	8	88	X	120	x
57	9	89	Y	121	y
58	:	90	Z	122	z
59	;	91	[	123	{
60	<	92	\	124	|
61	=	93	]	125	}
62	>	94	^	126	~
63	?	95	_	127	

1.10 SYSTEM-80 DETAILED MEMORY AND I/O MAP

Here is a map showing most of the important Memory and I/O space addresses for the System-80 computer. Both decimal and hexadecimal addresses are given for your convenience.

ADDRESS		SIGNIFICANCE
Decimal	Hexadecimal	
0	0000	Start of Level II BASIC ROMs
12287	2FFF	End of ROM space
12288-13823	3000-35FF	Custom EPROM (if fitted)
13824-14303	3600-37DF	Unoccupied
14304	37E0	Interrupt latch address
14305	37E1	Disk drive select latch addr.
14316	37EC	Disk controller address
14336-15359	3800-3BFF	Keyboard matrix addresses
15360-16383	3C00-3FFF	Video refresh memory
16384-16402	4000-4012	Start of RAM -- RST vectors
16405	4015	Keyboard device control block (4016/7 are used to store the calling addr. of keyboard driver routine)
16413	401D	Video display control block (401E/F are used to store the calling addr. of video driver routine, 4020/1 to store the cursor position)
16421	4025	Line printer control block (4026/7 are used to store the calling addr. of the printer driver routine, 4028 stores the lines/page, and 4029 the number of lines printed on the current page)

16464	4Ø5Ø	Disk cont. interrupt vector
16466	4Ø52	Communications int. vector
16548-16549	4ØA4-4ØA5	Ptr to start of BASIC program
16561-16562	4ØB1-4ØB2	Ptr to top of BASIC memory
16598-16599	4ØD6-4ØD7	Memory size stored here
16607-16608	4ØDF-4ØEØ	Ptr to entry address for SYSTEM programs
16620-16621	4ØEC-4ØED	EDIT line number
16629-16630	4ØF5-4ØF6	Last line number executed
16637-16638	4ØFD-4ØFE	Free space size
16870-17127	41E6-42E7	I/O buffer area
17128	42E8	Always zero
17129	42E9	Normal start of a BASIC program. Text is stored first, then simple variables and arrays. String space and stack are stored downwards from the top of memory, or from the bottom of any space at top of memory which has been reserved for machine language routines
20479	4FFF	End of 4K RAM
32767	7FFF	End of 16K RAM
49151	BFFF	End of 32K RAM
65535	FFFF	End of 48K RAM

I/O ADDRESSES

248	F8	RS232 port (data in/status out)
249	F9	RS232 port (data out/status in)
253	FD	Printer port address
254	FE	Int/ext cassette latch (bit4)
255	FF	Cassette data port

HEX-TO-DECIMAL CONVERSION CHART

HEX CODE	Most Significant Bytes		Least Significant Bytes	
	IV	III	II	I
0	0	0	0	0
1	4096	256	16	1
2	8192	512	32	2
3	12288	768	48	3
4	16384	1024	64	4
5	20480	1280	80	5
6	24576	1536	96	6
7	28672	1792	112	7
8	32768	2048	128	8
9	36864	2304	144	9
A	40960	2560	160	10
B	45056	2816	176	11
C	49152	3072	192	12
D	53348	3328	208	13
E	57344	3584	224	14
F	61440	3840	240	15

For each hexadecimal digit, go down the hex code column at the left until you find the right digit. Then move across to the right column. When all four digits have been converted into their decimal equivalents I, II, III, IV, add these all together to get the final answer. I.e.,

Decimal Value = IV + III + II + I

2. TROUBLESHOOTING

2.1 INTRODUCTION

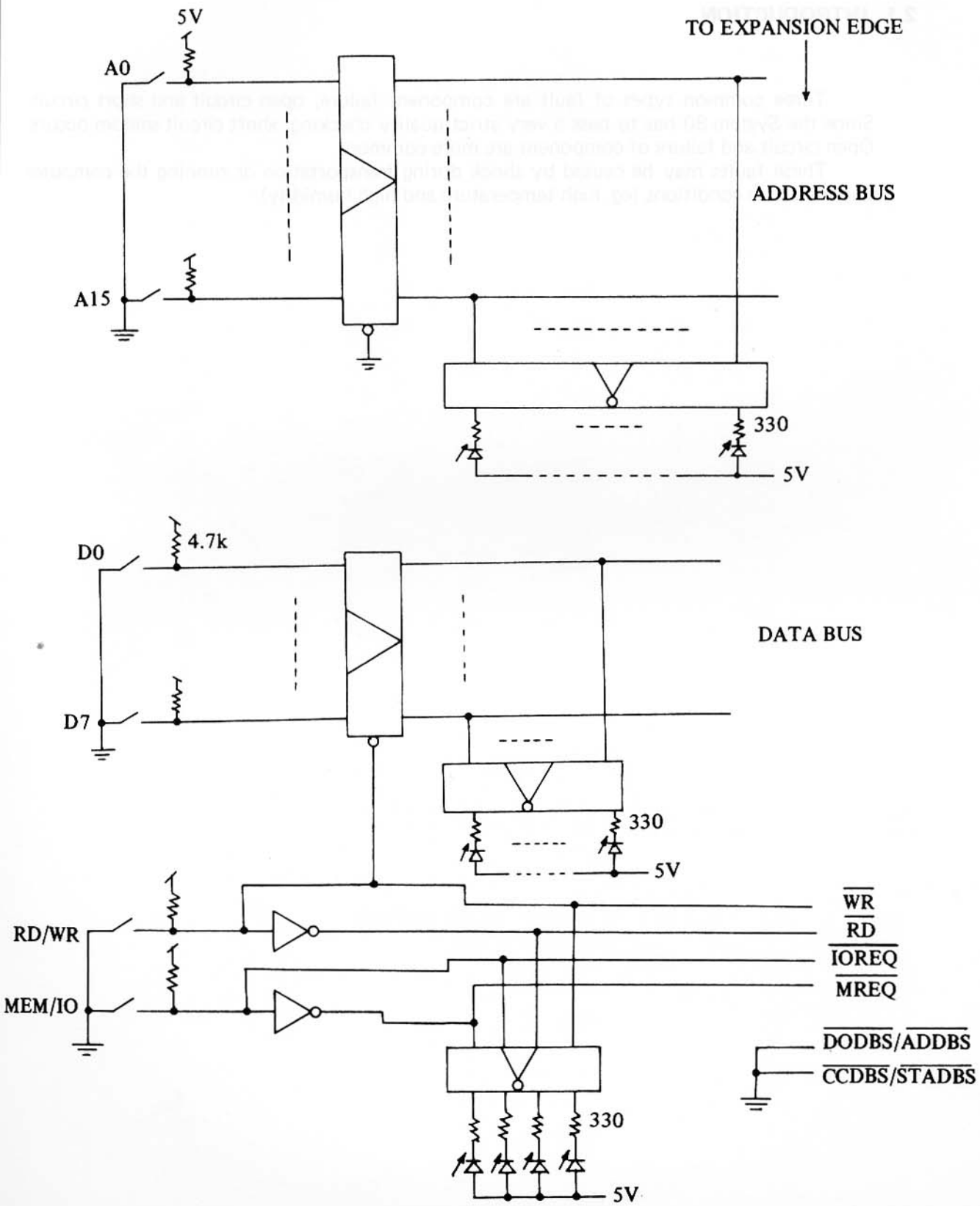
Three common types of fault are component failure, open circuit and short circuit. Since the System-80 has to pass a very strict quality checking, short circuit seldom occurs. Open circuit and failure of component are more common.

These faults may be caused by shock during transportation or running the computer under adverse conditions (eg. high temperature and high humidity).

2.2 BUS CHECK – DATA, ADDRESS AND CONTROL BUSES

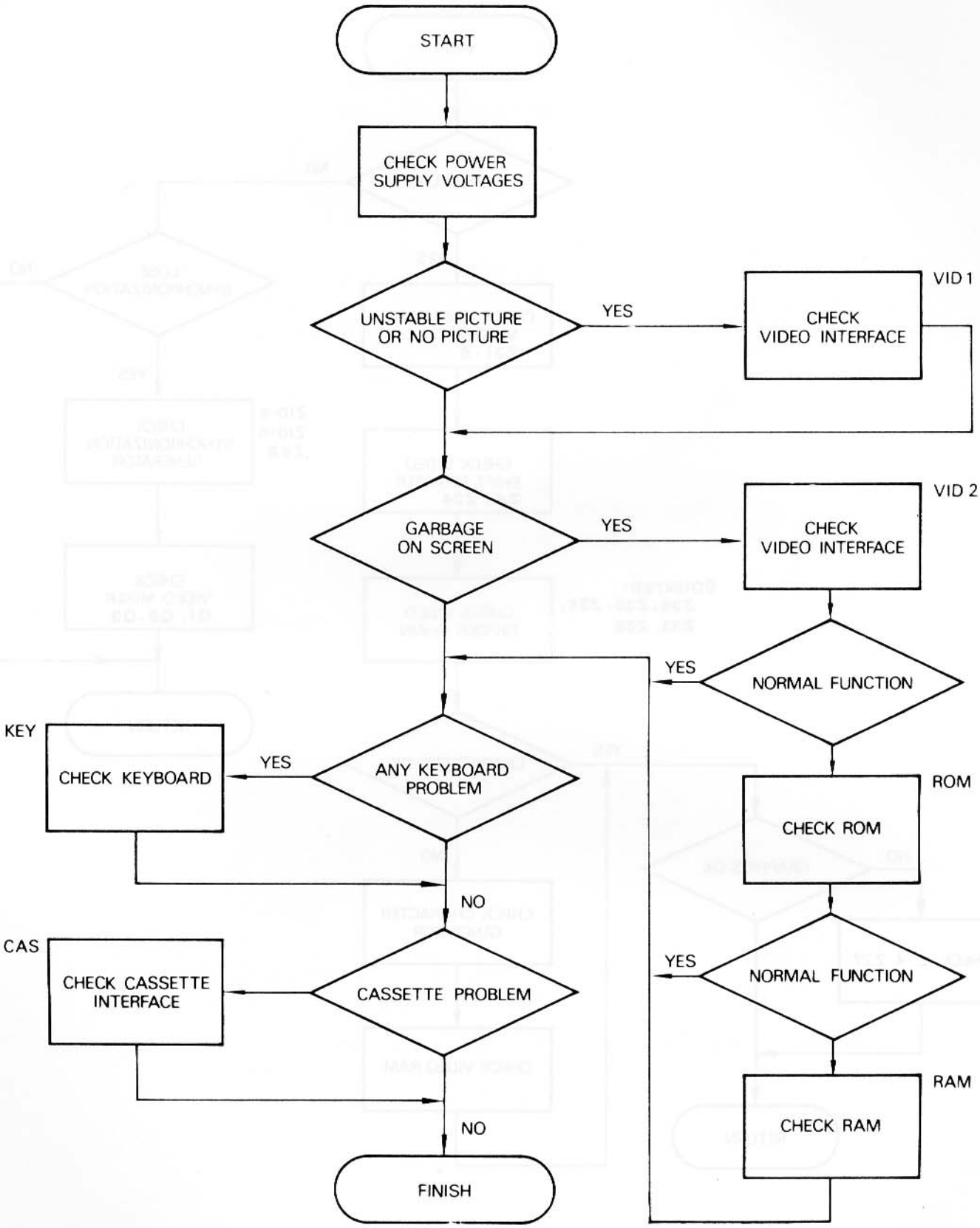
Bus check can be facilitated by a simple tester. It disables the CPU buffers and puts data, address and control signals on the buses. Therefore, short circuits and open circuits can be tested under static condition.

Fig. 2.1 TESTER CIRCUIT DIAGRAM



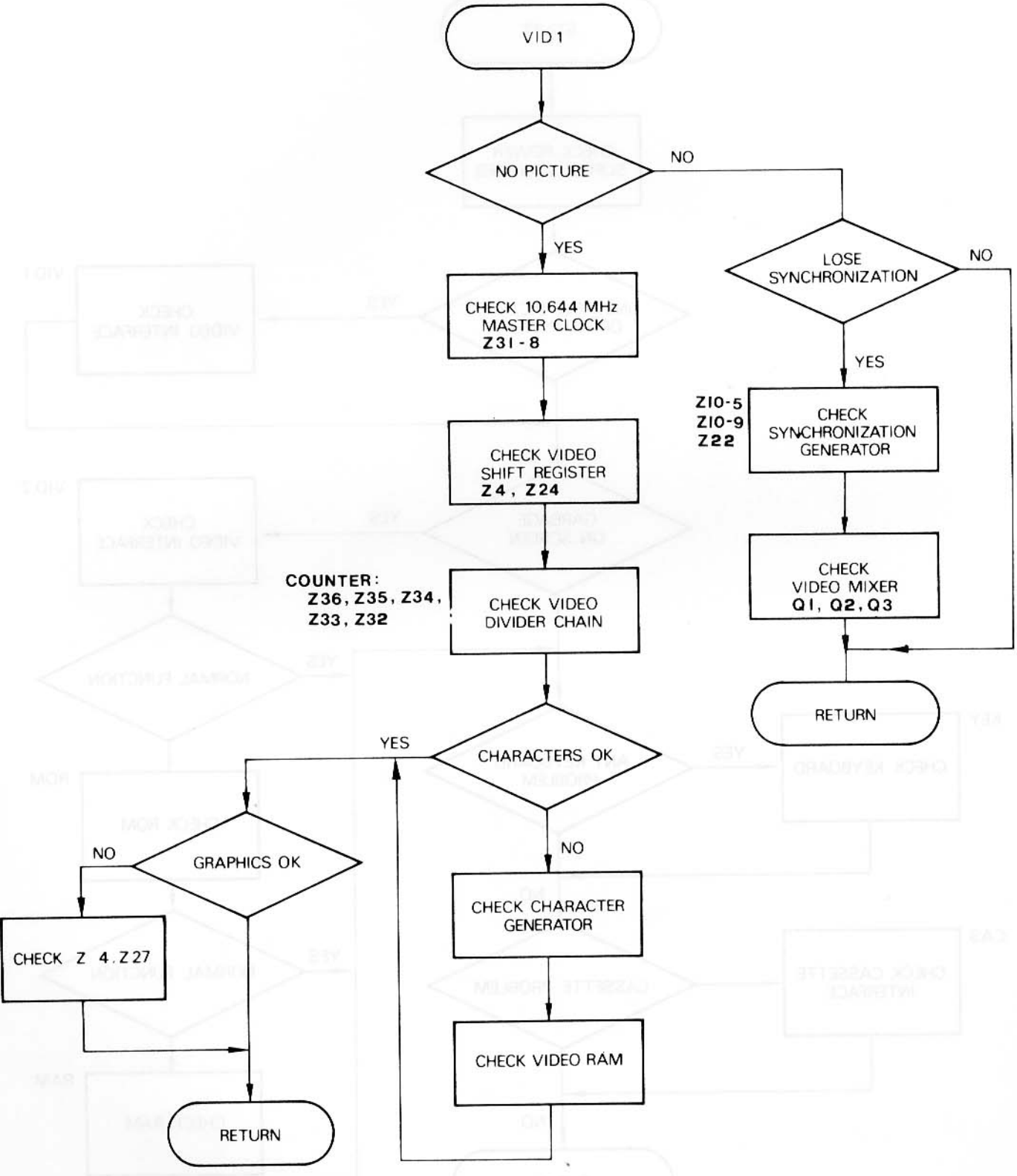
2.3 TROUBLESHOOTING FLOWCHARTS

General Flowchart in Troubleshooting

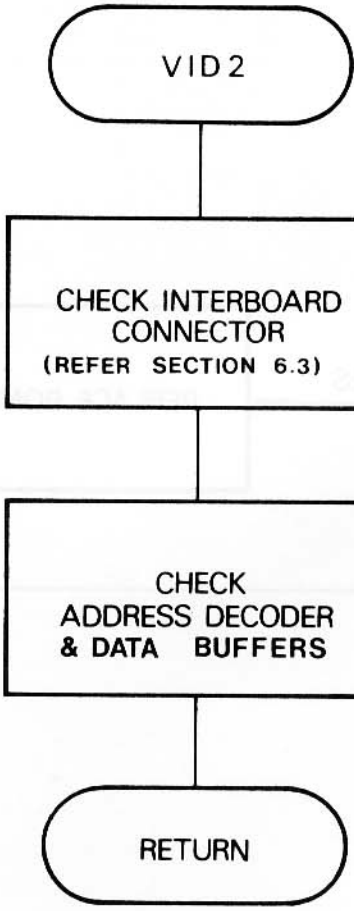


2.3.1 Video Interface

(Interface Board)



(Interface Board)



DECODER : Z30 , Z39 , Z38

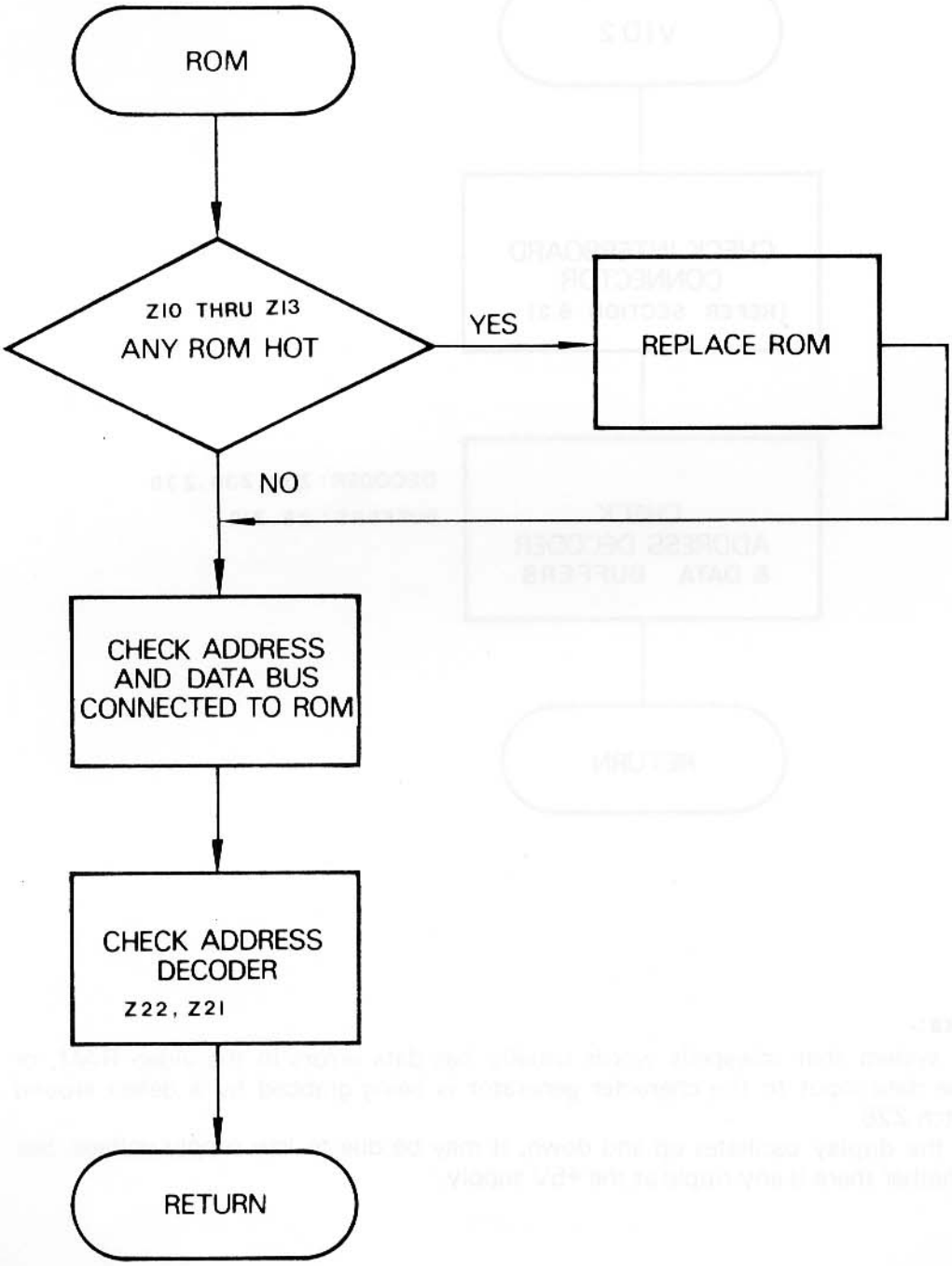
BUFFERS : Z5 , Z12

Remarks :-

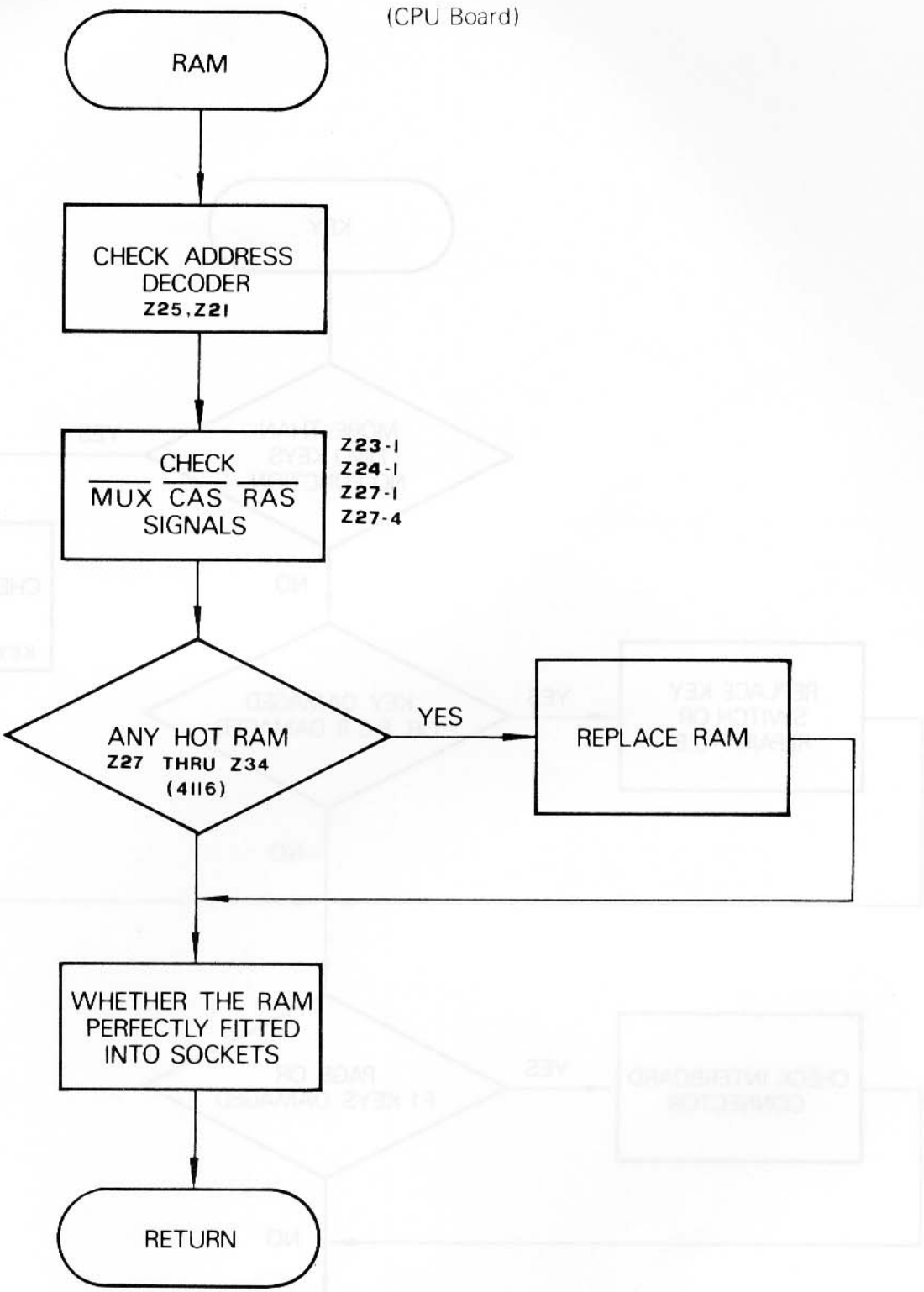
1) A system that mis-spells words usually has data errors in the video RAM, or the data input to the character generator is being grabbed by a defect around latch Z26.
2) If the display oscillates up and down, it may be due to low supply voltage. See whether there is any ripple at the +5V supply.

2.3.2 System ROM's

(CPU Board)



2.3.3 User RAM

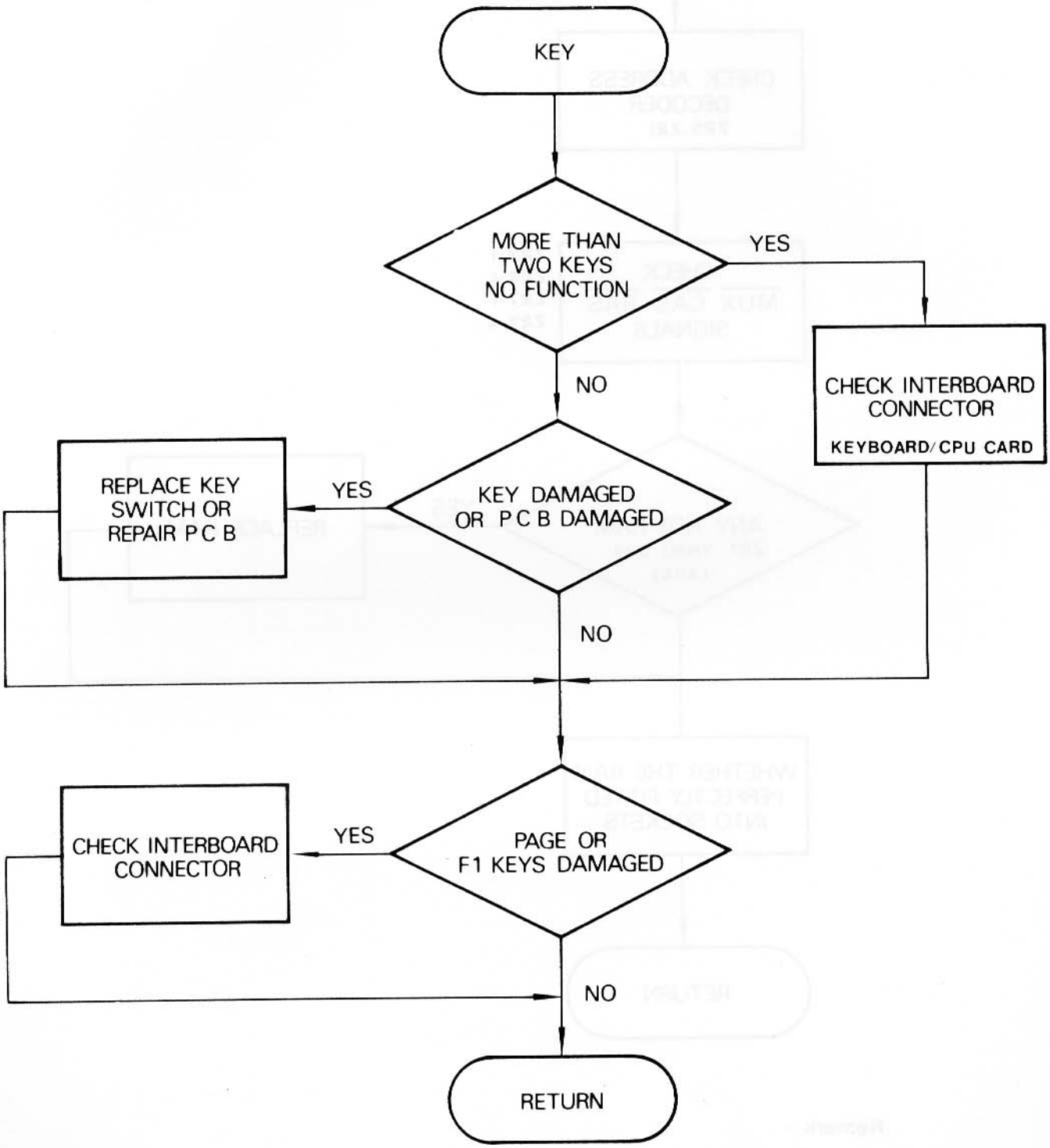


Remark :-

The flowcharts of RAM and ROM checking seems quite simple, but actually it is most difficult to determine whether the component is damaged. The best way to check these sections is to replace the RAM or ROM chips with good ones if other sections of the circuits are working normally.

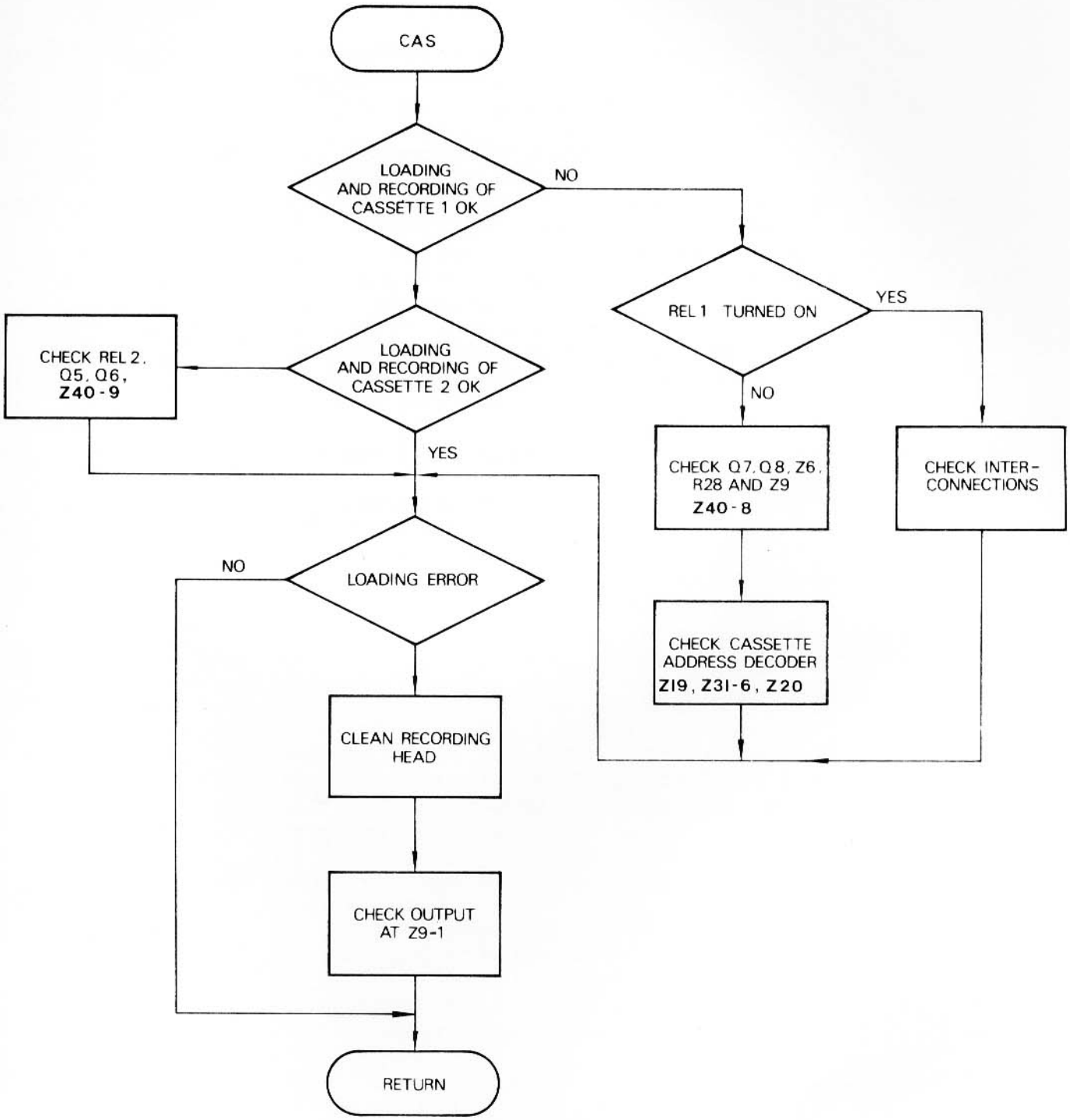
Precaution : CPU, ROM and RAM chips should be placed on conductive materials after taking out from the circuit.

2.3.4 Keyboard



2.3.5 Cassette Interface

(Interface Board)



Remark· Sometimes, cassette loading error may not be caused by circuit fault, but due to the poor quality of the cassette tape.

3. TROUBLE-SHOOTING HINTS

KEYBOARD MALFUNCTIONS

Symptom — Keyboard has bounce

Probable Fault
i) Incorrect typing style
ii) Keyswitch bounce

Cures
i) Adjust typing technique to overcome bounce - generally your technique should be slower than that used on a conventional electric typewriter, due to the scan rate of the System 80 keyboard.
ii) Replace offending keyswitch by removing keyboard, desoldering keyswitch and replacing with new keyswitch.

Symptom — Keyboard not operating

Probable Fault — Keyboard connector dislodged

Cure — Remove cover, re-insert ribbon cable into connector on keyboard. Ensure that no wires are bent or broken.

Symptom — One key not working

Probable Fault — Dry joint or broken track on keyboard

Cure — Remove cover and 8 keyboard retaining screws, examine circuit board under faulty key, resolder and test for continuity and correct switch operation.

Symptom — Several keys not operating on keyboard

Probable Fault
i) Ribbon connector with wire/s broken on circuit board due to fatiguing.
ii) Ribbon cable not slotting into keyboard connector correctly.

Cure
i) Refer to circuit diagram. Keys will probably be related by either the horizontal or vertical matrix. Examine the ribbon connection on the CPU board and reterminate any broken wires with a soldering iron. If this does not cure the problem, remove the keyboard and check for continuity along the copper tracks. Resolder any breaks or dry joints as necessary.
ii) Check that cable is slotted into keyboard.

VIDEO ABSENT OR IRREGULAR

Symptom

No video on screen when used on TV monitor, power indicator on cassette working.

Probable Faults

i) Video cut switch and page key depressed - monitor displays RHS of screen only.

ii) Monitor at fault.

iii) Lead from computer to monitor plugged into tape instead of video or loosely installed.

iv) Video output transistor in computer faulty.

v) Cable or RCA plug at fault.

Cures

i) Check and put keys in appropriate settings.

ii) Try computer on another monitor or TV.

iii) Check connections to TV and Computer. Computer end of cable can be particularly hard to insert. Exchange components to isolate faulty component.

iv) Remove cover from computer and locate Q3 on circuit board. Q3 is the transistor closest to the 5-pin socket. Using a multimeter on the lowest ohms scale, check the emitter to collector resistance of the transistor in both directions. If it appears to have low resistance (in the order of 30ohms) in both directions, then it is likely to be short circuited. This transistor can be readily replaced with a DS549 (Note pin orientation) The flat on the transistor will face the rear of the computer.
If the computer is still faulty, return the unit to your System 80 agent for service.

v) Try another cable.

Symptom

Video on screen wavering in slow snaking motion

Probable Fault

i) Diodes in power supply faulty.

ii) Capacitor in power supply faulty.

iii) Monitor receiving magnetic interference from another appliance.

Cure

i) Replace two largest diodes in power supply box with IN5408 diodes.

ii) Replace 22000microfarad capacitor with new one. Also check for broken tracks under capacitor. Secure capacitor body to PCB with rubberized glue.

iii) Remove monitor from influence of other appliances.

Symptom — No video LED, indicator off.

Probable Fault
i) Power supply unplugged

ii) Power supply not operating.

iii) Regulator/s faulty.

Cures
i) Ensure that the power supply is plugged into the mains socket properly. Remove the lid from the computer and ensure that the lead going from the power supply box to the CPU board is plugged in at both ends. Check for broken wires.

ii) Check fuse on rear of computer. Measure output of power supply for +8V, +16V and -16V with respect to ground. A handy grounding point is the negative side of the 22000microfarad electrolytic in the PSU. If any of these voltages is absent check the AC outputs of the two transformers. Replace if necessary. Also test the input voltages to the 7812 and 7805 regulators.

iii) Check the output voltage of the 7805 regulator on the CPU board. It should measure 5V. This is most easy to acheive by measuring across diode 3 on the CPU board. If there is no voltage or a lower voltage than 5V, suspect the regulator or a short circuit on the 5V rail. Isolate the output of the 7805 IC regulator from the rest of the circuit and measure the output voltage again. If the voltage is now 5V, then the fault is elsewhere in the circuit and the unit should be returned to your dealer.

PICTURE POSITION ADJUSTMENT

After the video interface has been serviced, the picture position should be adjusted so as to make the picture balanced in the centre of the screen.

Enter and run the following simple program. A rectangle showing the screen boundary will then be drawn. VR1 and VR2 should be adjusted with a non-metallic screwdriver.

```
10   CLS
20   FOR X=0 TO 127
30   SET(X,0):SET(X,47)
40   NEXT X
50   FOR Y=0 TO 47
60   SET(0,Y):SET(63,Y):SET(64,Y):SET(127,Y)
70   NEXT Y
75   PRINT @522,"LEFT";:PRINT @554,"RIGHT",
80   GOTO 20
90   END
```

CASSETTE MECHANISM NOT WORKING

Symptom — Cassette light comes on but cassette does not turn

Probable Fault
i) Cassette drive belt broken or run off flywheel or pulley.
ii) Power regulating transistor faulty.
iii) Relay not operating or contacts faulty

Cure
i) Remove cassette mechanism and inspect drive belt. Correct as necessary. If the mechanism appears to be O.K., turn the pulley or flywheel to check free movement of the mechanism. If the mechanism is jammed manipulation should free it.
ii) Replace Q10 with a TIP31B transistor. Note orientation of the new transistor is the same as the original.
iii) Replace relay as necessary.

MODIFICATIONS TO IMPROVE CASSETTE RELIABILITY

1. In some units Q9 (on Interface Board) has been deleted and a wire link substituted between collector and emmitter. This drops the output from the regulator Q10 by 1.5V. In these units change zener diode Z1 from 8.2 to 10V. This will improve cassette loading.

2. For optimum performance from the cassette loading circuitry, C1 (0.0047uF) on the cassette amplifier board (located below the cassette mechanism) must be changed to 0.047uF. In addition C5 (0.1uF) should be changed to 0.27uF.
   Note: All Blue Label computers and some earlier models are factory fitted with the correct value components.

CASSETTE LOADING DIFFICULTIES

Symptom — Cassette not loading - asterisks staying on. (Basic tapes only)

Probable Fault
i) Cassette volume set too high.
ii) Cassette heads out of alignment.

Cure
i) Reduce volume level and repeat loading procedure until volume setting causes asterisks to flash.
ii) Realign heads by either method outlined below.
1) Remove the computer lid and locate the green wire and its associated harness of red black and yellow wires leading away from the cassette deck to the four way connector on the Interface Board. Earth oscilloscope lead to the metal tab of the 7812 regulator and place the probe into the connector socket of the green wire. While monitoring the output waveform on the oscilloscope, gently insert a

small Philip's head screwdrive into the left hand spring loaded screw fastening the cassette playback head. Applying minimal downwards pressure, slowly rotate the screw up and down until maximum amplitude is obtained on the oscilloscope. Once this has been acheived, apply a small dab of nail polish to secure the head of the screw. .
Note : Use a commercially recorded computer cassette to align heads, otherwise there will be great difficulty in loading tapes not recorded on the computer.

2) Remove the lid from the computer. Insert and play a high quality, commercially recorded computer cassette in the deck. While monitoring the signal meter in the computer insert a small Philips's head screwdriver into the left hand spring-loaded screw fastening the playback head. Adjust screw, applying minimum downward pressure, until maximum reading is obtained. Lock screw in position with a small dab of nail polish to prevent head vibrating out of alignment.

Symptom — Cassette not loading. Left hand asterisk changing into a "C". (System tapes only)

Probable Fault
i) Insufficient volume.
ii) Dirty or magnetized heads.
iii) Heads out of alignment.

Cure
i) Increase volume level and reload so that asterisks flash normally.
ii) Gently clean the surface of the playback head with a cotton wool bud immersed in an alcohol solution. Demagnetise playback head using a cassette demagnetising tool.

Symptom — Asterisks flash normally and program appears to load successfully until run. When run or listed, numerous errors are discoverd in the program.

Probable Fault
i) Faulty cassette, either poorly saved or corrupted.
ii) Cassette playback head out of alignment.

Cure
i) Try another prerecorded cassette to determine where the fault lies i.e. in the cassette or in the computer's cassette player.
ii) Re-align heads as outlined in preceding section concerning asterisks staying on while loading from cassette.

Symptom — Cassette loading intermittent.

Probable Fault
i) Dry joint on cassette board.
ii) Alignment problems.
iii) Capacitors dry.

Cures
i) Remove computer lid and undo the five retaining screws holding the cassette deck and associated meter into the case. Unplug the cassette harness and turn the deck over to reveal the circuit board. Remove the two retaining screws and turn the board over - component side up. Check all component leads to ensure proper connection.
Visually examine all leads connected to the board for short or open circuits. Turn the circuit board over and resolder any suspicious looking joints, reassemble and test.
Note : Do not use to much force to pull wires.

ii) Realign heads as outlined in previous section - "Cassette loading but asterisks not flashing".

iii) Intermittent loading may be a result of dry electrolytics in the cassette circuitry. Replacement of the following electrlytics in the cassette circuit will overcome faults attributable to dry electrolytics. Replace C7, 10uF with a 47uF 16V electrolytic.
Note: Observe correct polarity for electrolytics - refer to Manual if unsure!

Symptom — Cassette loads but program will not run. If listed program lines are all rubbish.

Cure — Reload program and turn the volume on the cassette deck up one notch.

Symptom — Information being displayed changes at random. Similarly graphics characters appear at the bottom of the screen. Another symptom is that the READY display will change cnaracters e.g. ŒADY, PEADY, READ etc.

Probable Fault — Screen RAM is faulty - these are either 21L02 or 2114's depending on your machine.

Cure — Remove cover and keyboard. Screen RAM IC's are located on the right hand side and are located in a vertical row. Rather than changing all eight (21L02), try changing two at a time.

SCREEN DISPLAYING "S's" & "0's"

Symptom — Computer shows "S's" and "0's" on entire screen and will not clear.

Probable Fault
i) Faulty RAM.
ii) 12V supply rail faulty.
iii) Fault somewhere other than RAM or CPU board.

Cure
i) Check all RAM and determine whether any IC's are abnormally hot. Exchange RAM for new IC's to check if RAM is faulty.
Use only prime spec 4116 type Dynamic RAM's of 250nS or faster access time. These are available at Dick Smith stores (Cat.No: Z9310)

ii) Check +12V rail on RAM IC's. Check +5V and -12V rails as well. Ensure that the 0.1uF bypass capacitors across the 12V rail of the memory IC's are not short circuited.

iii) Exchange ROM. If the fault still prevails, return computer to Supplier for servicing.

SCREEN SHOWING GARBAGE

Symptom — Screen shows garbage at switch on and will not clear.

Probable Fault
i) Insufficient time given for power supply to discharge when computer was switched off.
ii) Connection between CPU board and Interface board either broken or some wires unplugged.
iii) Faulty RAM, ROM or CPU.

Cure
i) Allow at least 30 seconds after switching computer off.

ii) Inspect connector cables between CPU board. Resolder any broken terminations. Reinsert any unsocketed wires.

iii) Ensure that all ROM, RAM and CPU IC's are properly inserted. Check that no pins ar bent under the IC's. Methodically replace RAM, ROM and CPU.
If the fault still persists we suggest you return the computer for servicing.
Note: In some cases it may be necessary to hold BREAK and press RESET together to reset the computer. If this happens when the computer is not connected to an Expansion Unit, then it is an indication that the data bus is being unduly loaded. To test this try reading from an unused address - e.g.PRINT PEEK(-16384). The result should always be 255 (0FFH) i.e. all data bits floating high.

PROGRAMS BEING CORRUPTED.

Symptom — Computer continually corrupts certain program lines.

Probable Fault

i) RAM faulty.

ii) ROM faulty.

iii) CPU faulty.

iv) Misloading of program.

v) Faulty tapes.

Cure

i) Test RAM using Dick Smith RAM/DISC Diagnostic Tests (Cat No: X-3763).

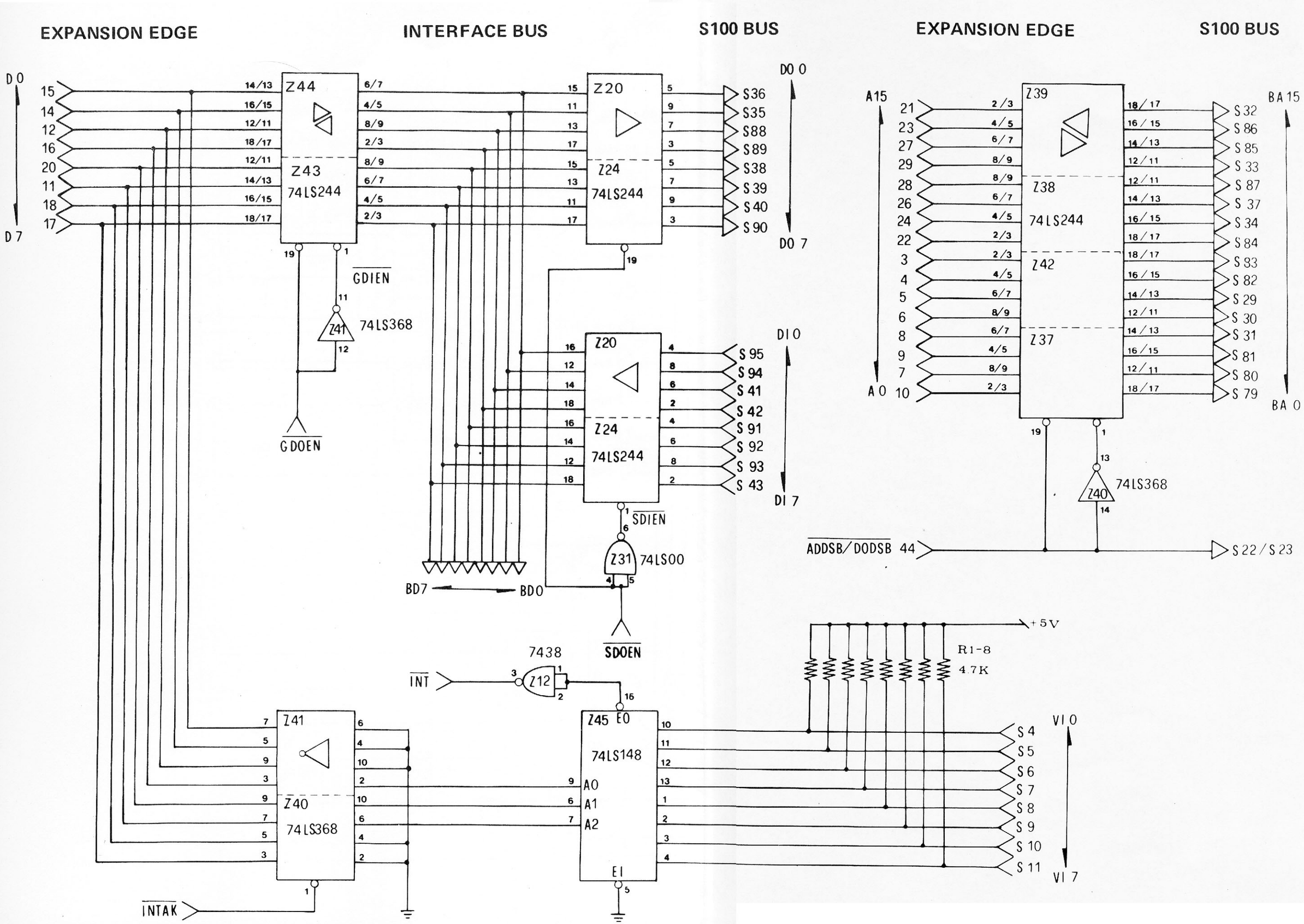
ii) Exchange ROM and test.

iii) Replace CPU and test.

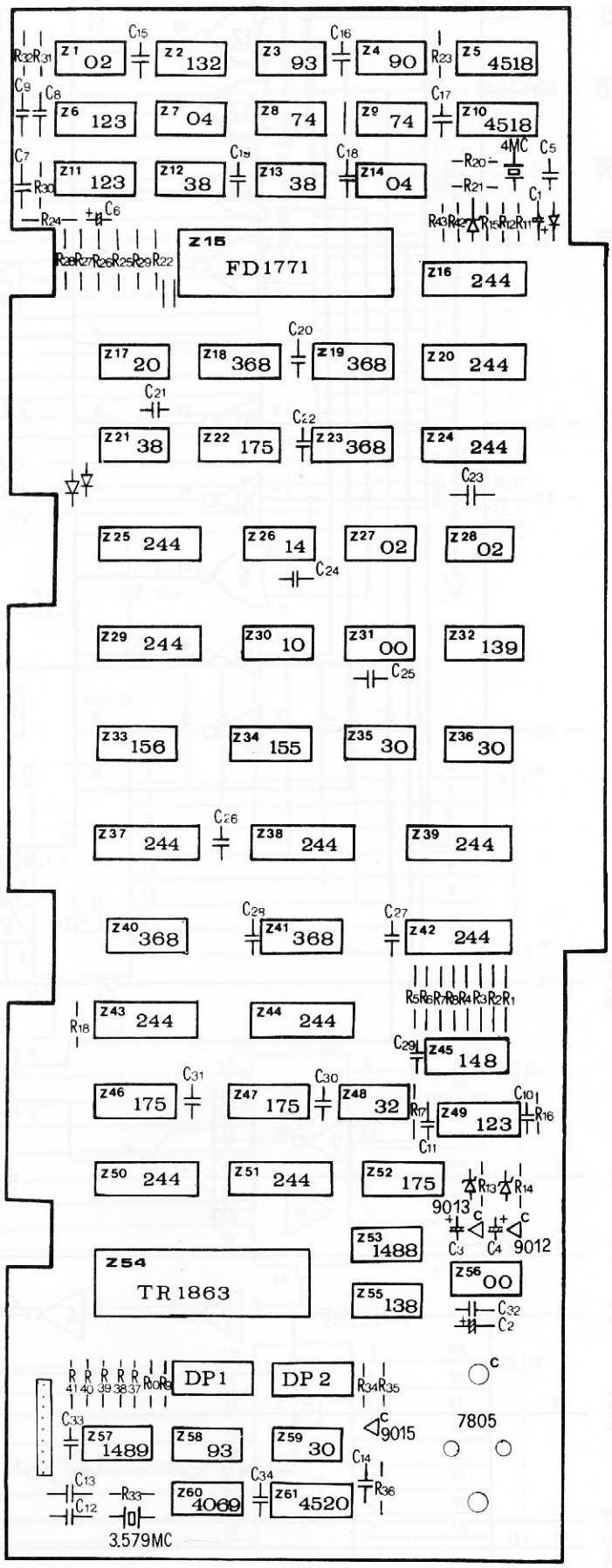
iv) See cassette loading errors section of manual.

v) Reload program using another cassette.

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.16	X-4010 EXPANSION UNIT INTERFACE BUFFERS



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.16	X-4010 EXPANSION UNIT INTERFACE BUFFERS



DICK SMITH SYSTEM 80	
DRAWING 4.15	*TITLE* X-4024 S-100 INTERFACE

EXPANDER

S100 BUS

MREQ – 47
RD – 48
WR – 39
ICRQ – 37
HALT – 35
MI – 45
PHLDA – 33
CCDBS / STATOBS – 41
FX – 6
INTA – 8
MEMDIS – 4
DODBS / ADDBS – 42
PINT – 34
RESET – 44
NMI – 43
PHANTOM – 36
PHOLD – 40

74LS14
74LS02
74LS05
74LS20
74LS04

MWRITE – 68
SMEMR – 47
SOUT – 45
SINP – 46
SWO – 97
SHLTA – 48
SMI – 44
SINTA – 96
PDBIN – 78
SHLDA – 26
PWR – 77
CDSB / SDSB – 18,19
ADSB / DOSB – 22,23
INT – 73
RESET – 75
NMI – 12
PHANTOM – 67
HOLD – 74

EXPANDER

S100 BUS

PHI – 31
RFRSH – 46
MREQ – 47
2MΦ – 2
BAΦ
BA15
8V – 5
16V – 1
-16V – 3

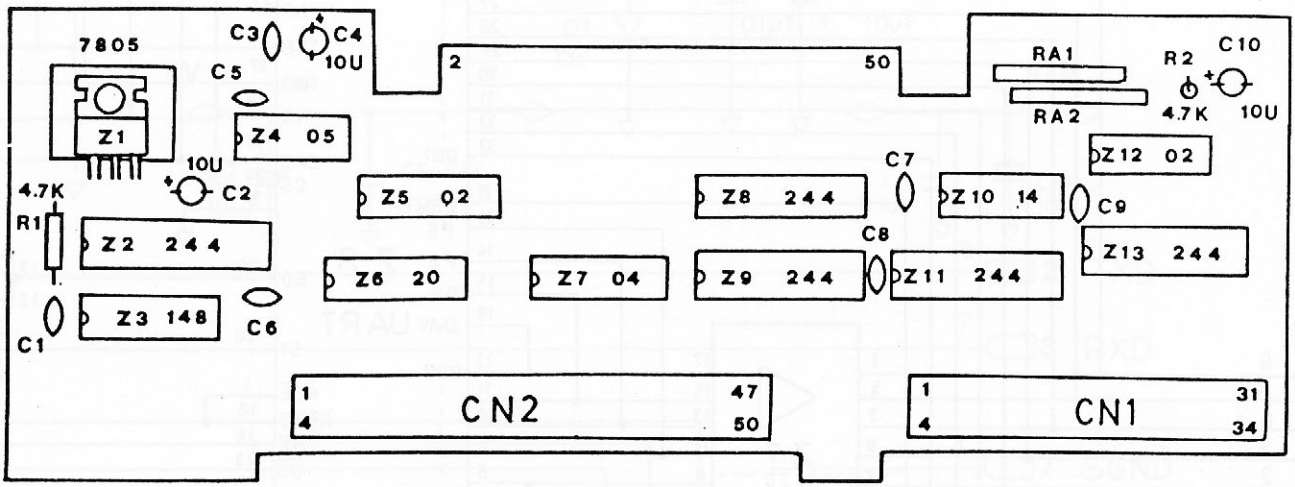
24 – Φ(B)
21 – SFRSH
65 – MREQ
49 – CLOCK(B)
79 – 80 – 81 – 31 – 30 – 29 – 87 – 83 – 36 – 34 – 37 – 87 – 33 – 85 – 86 – 32 – AΦ … A15
1,51 – 8V
2 – 16V
52 – -16V
99 – POC

Z1 7805
C1, C5-9 0.1u
C2 10u
C3 0.1u
C4 100u
C10 10u
R1 47K
R2 47K
R3-10 47K

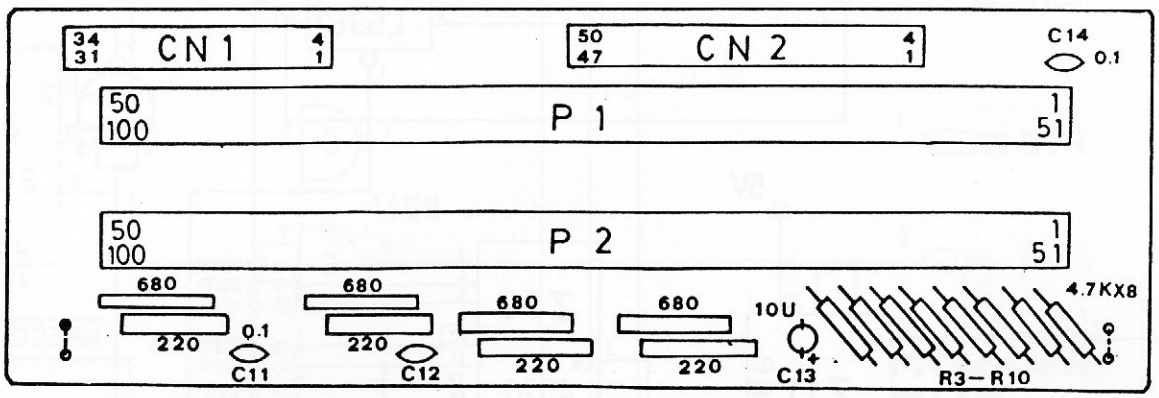
BDΦ … BD7
VIΦ* … VI7*
DOΦ … DO7
D1Φ … D7

74LS244

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.15	X-4024 S-100 INTERFACE

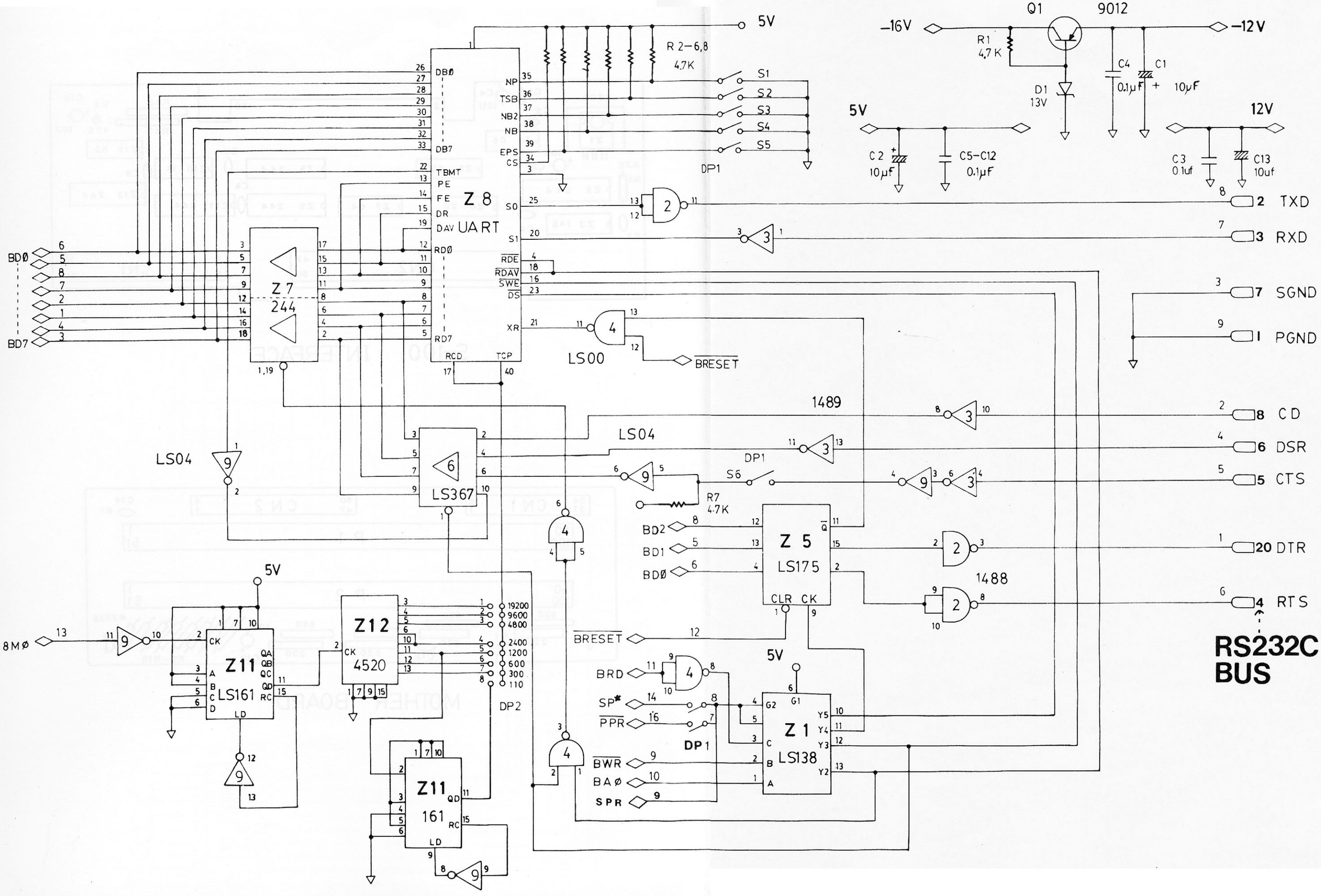


S-100 INTERFACE

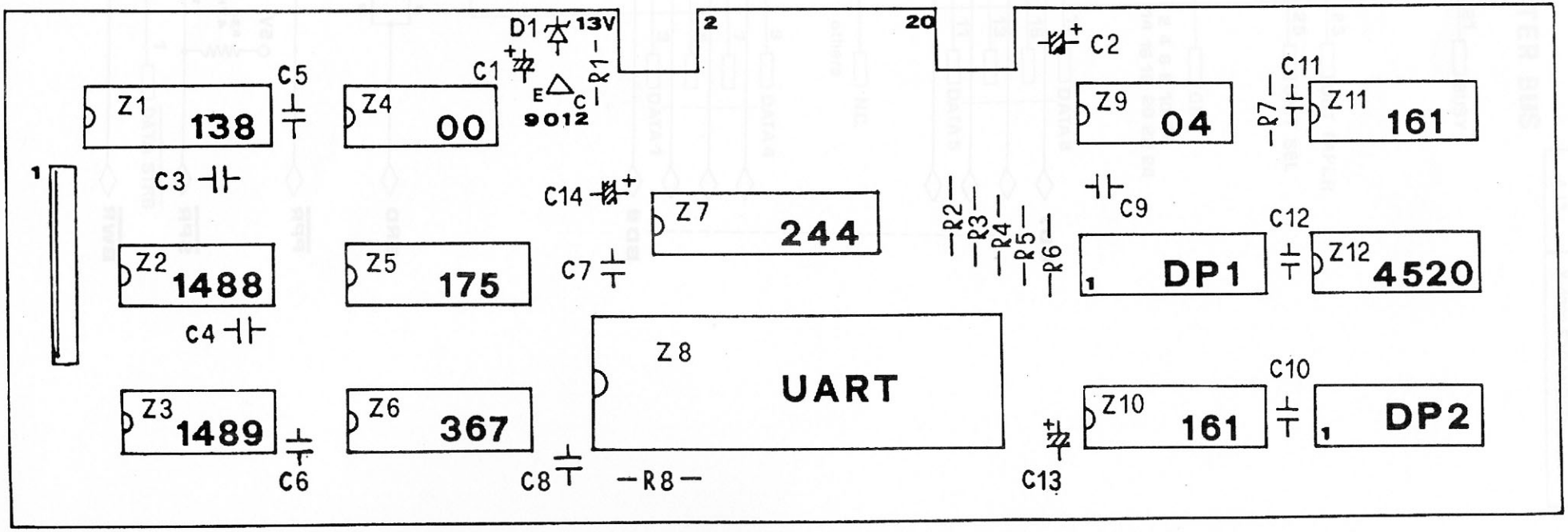


MOTHER BOARD

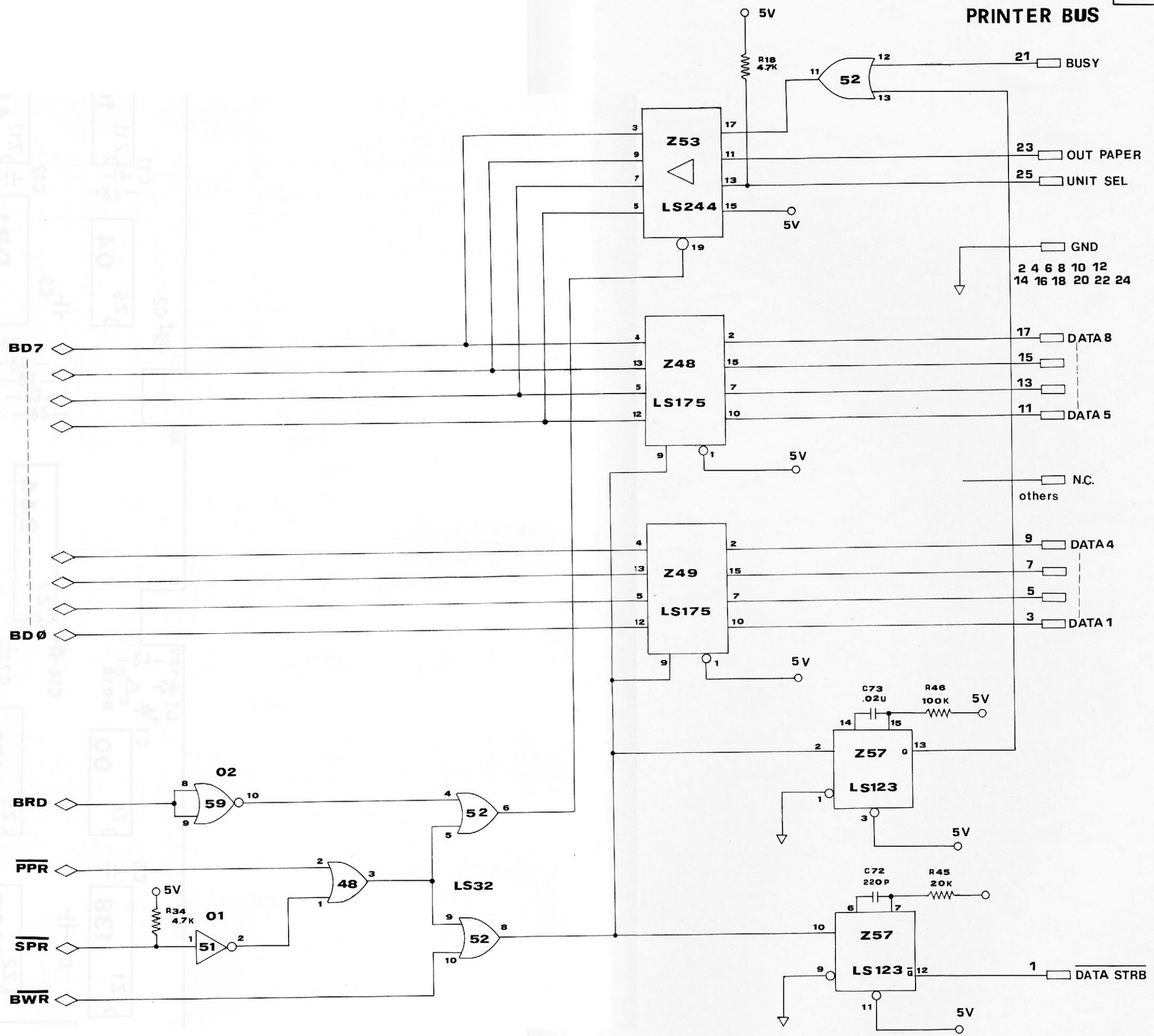
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.14	X-4022 RS-232C COMMUNICATIONS PORT



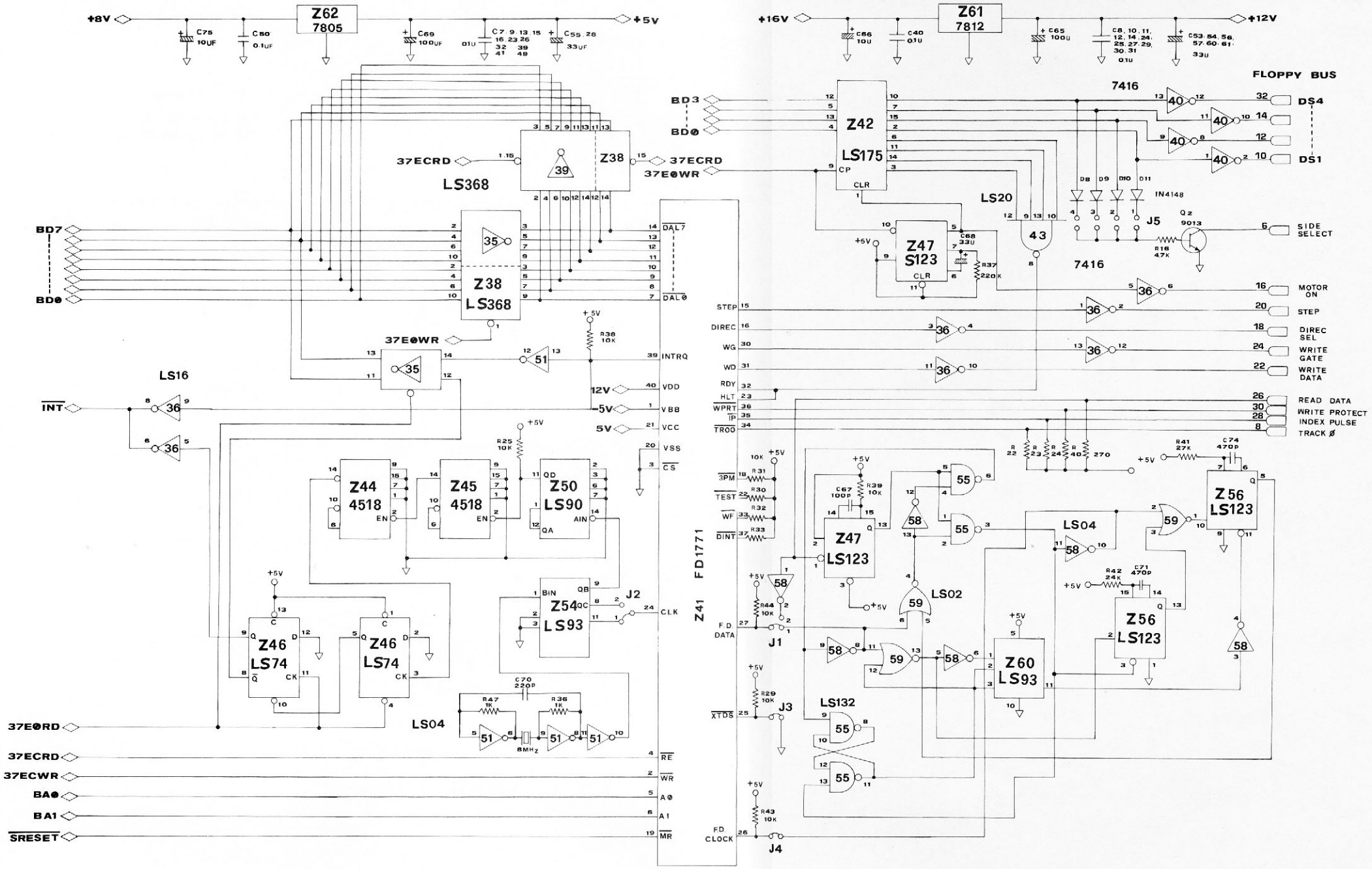
DICK SMITH SYSTEM 80	
DRAWING 4.14	TITLE X-4022 RS-232C COMMUNICATIONS PORT



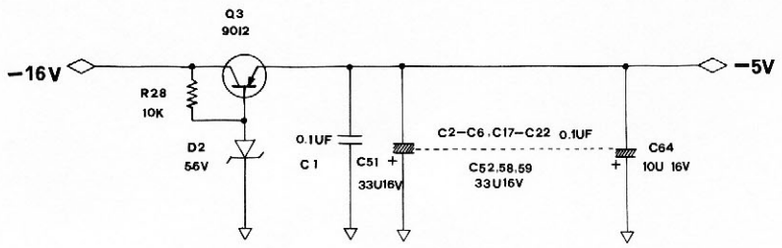
DICK SMITH SYSTEM 80	
DRAWING 4.13	*TITLE* X-4020 EXPANDER Sheet 4

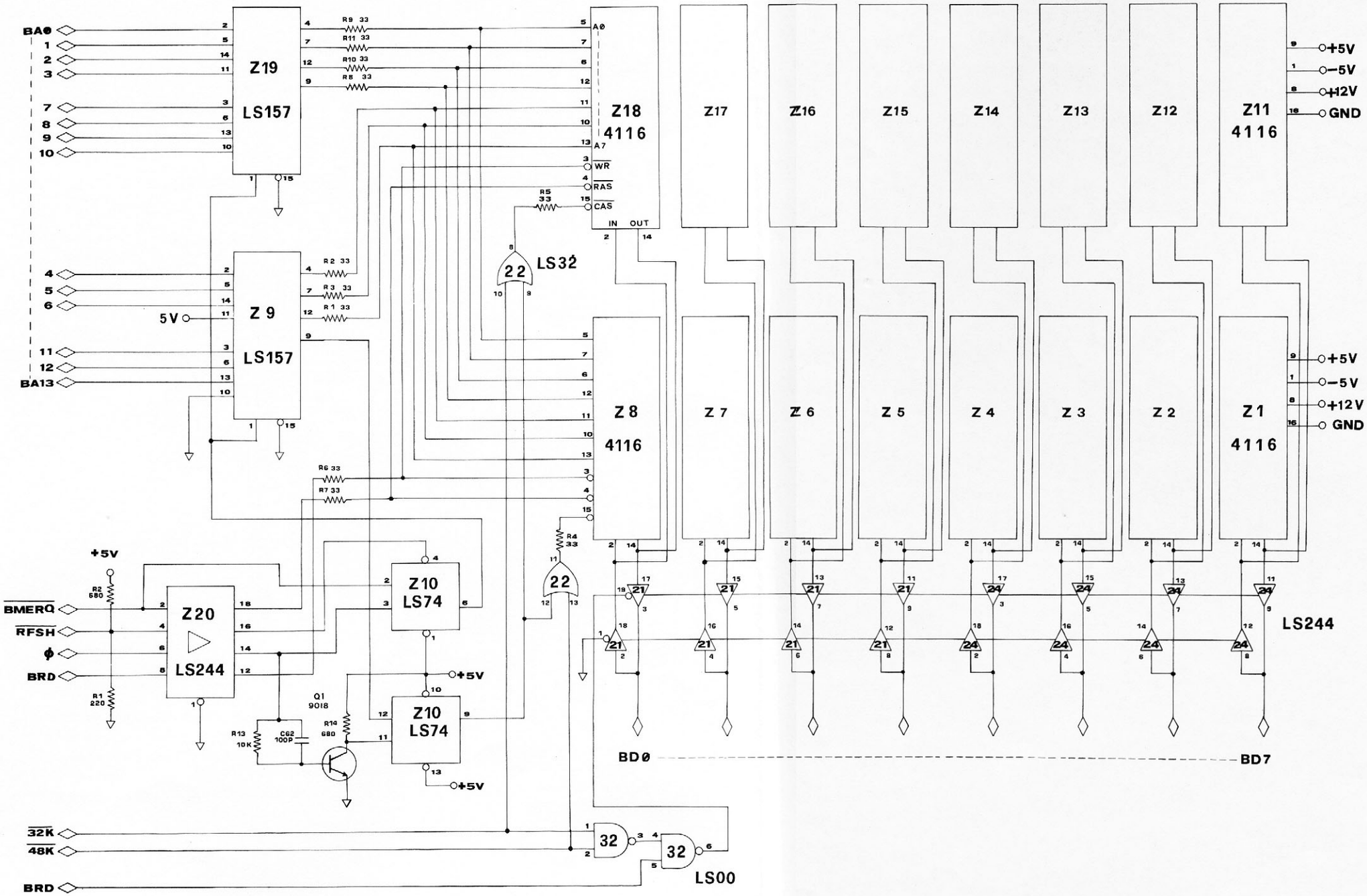


DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.12	**X-4020 EXPANDER** Sheet 3



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.11	X-4020 EXPANDER Sheet 2





DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.10	X-4020 EXPANDER Sheet 1

LS244

DO D7 BD0 BD7 Z28 Z30 DOEN 25

AO A15 BA0 BA15 680 220 Z33 Z26 ADDSB DODSB 25

LS244

IORQ MERQ RD WR BIORQ BMERQ BRD BWR CDBS SDBS Z20 25 BRD

BA4 BA5 BA6 BA7 BA8 BA9 BA10 BA12 BA13 LS30 23

BA11 BA14 BA15 Z29 LS139 +5V R15 4.7k

MEMDIS BMERQ 25 32 LS00

37EX BWR BA2 BA3 BRD Z34 LS155 37E0 RD 37E8 RD 37EC RD 37E0 WR 37E8 WR 37EC WR 32K 48K

+5v R18 R20 R19 R27 4.7k x4 D4 D3 1N4148 X 2

BA3 BIORQ LS30 27 BA2 BA1 BA0 Z31 LS156 SP PPR

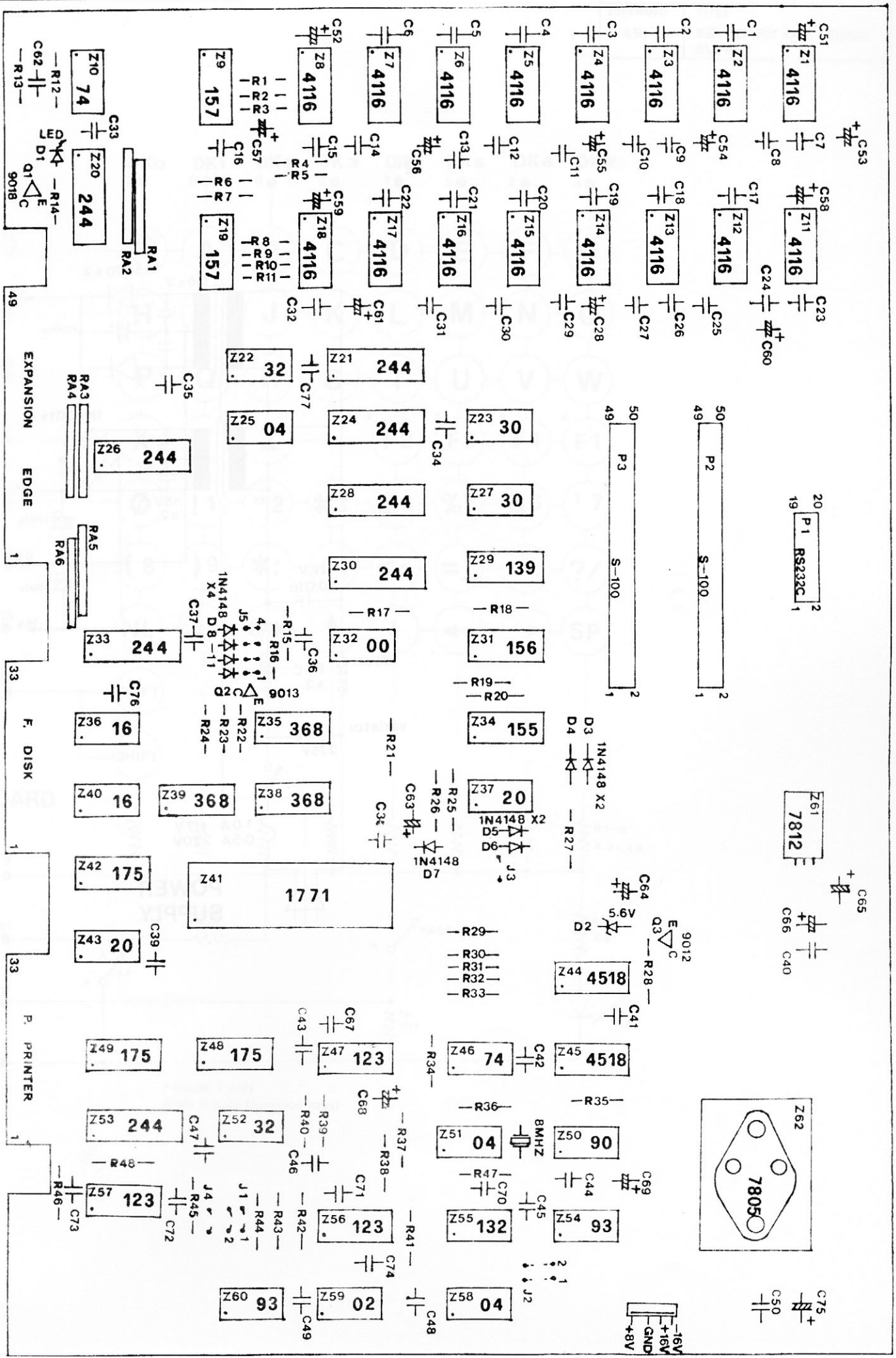
32K 48K 37EX BIORQ LS20 37 ADDSB DODSB BRD +5V R17 4.7k

INTA +5V R21 4.7k LS00 32 DOEN

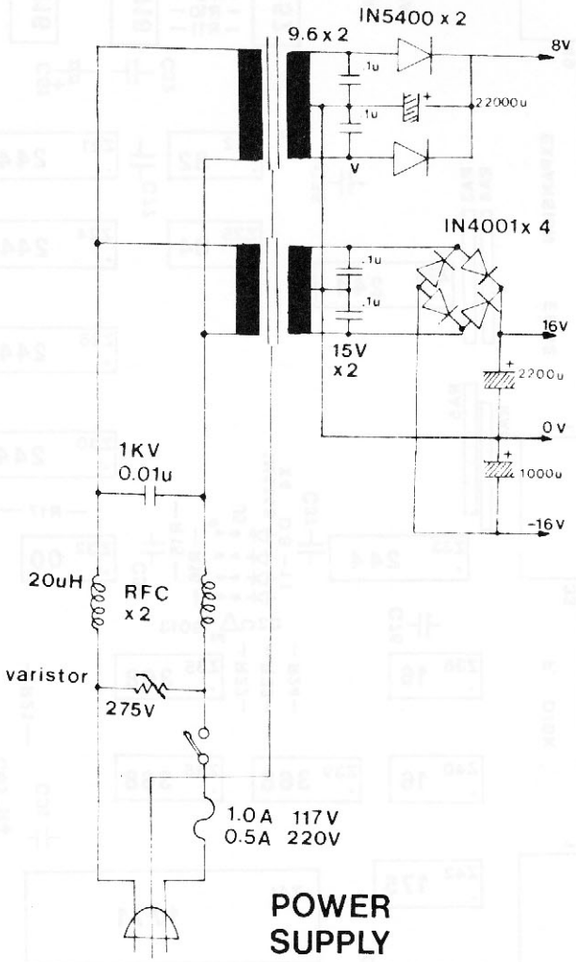
INTERNAL CON.
EXT. CONNECTOR
FROM EDGE

+5V R26 4.7k +5V R25 4.7k 1N4148 D5 D6 D7 NMI RESET SRESET C63 10 UF

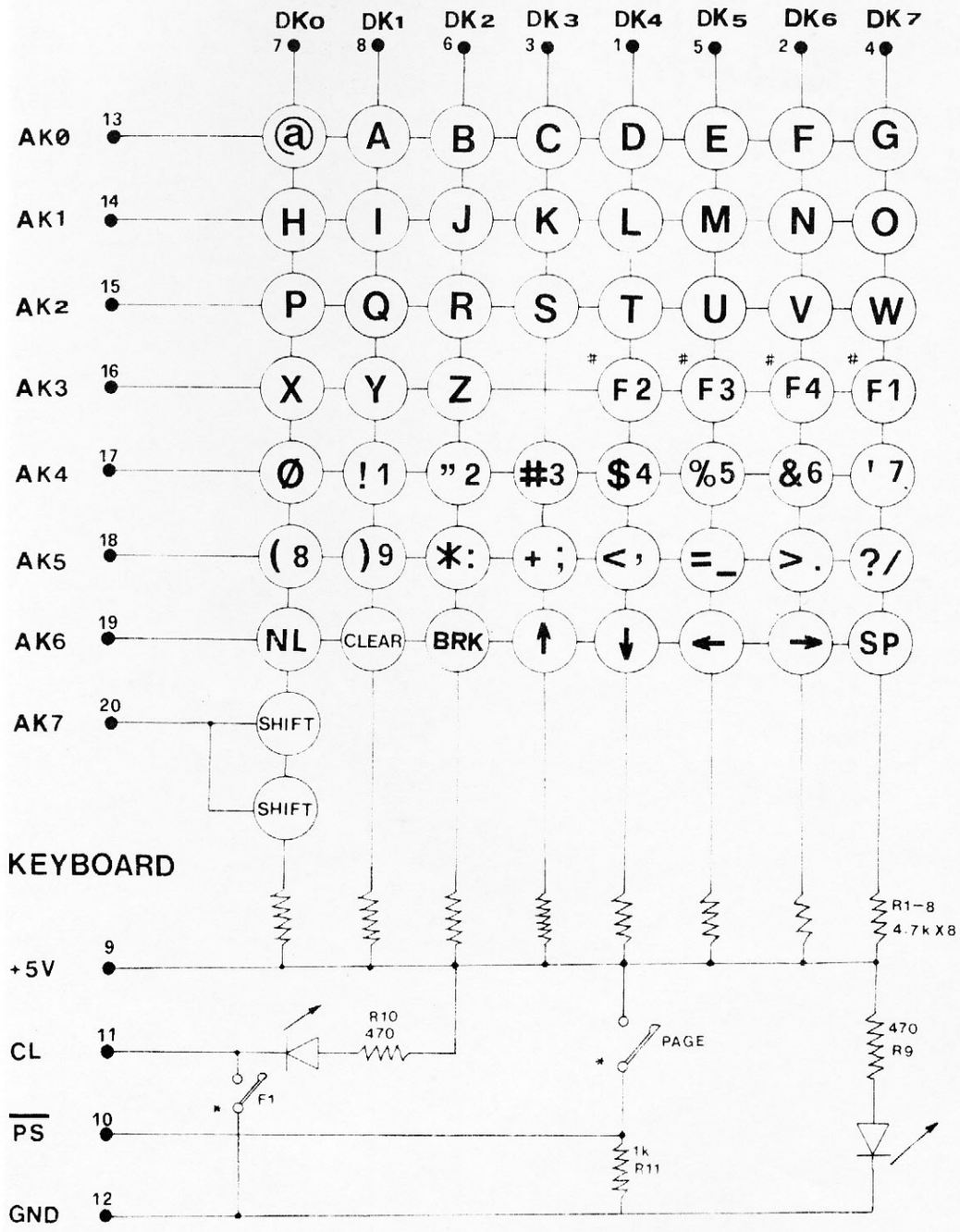
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.10	X-4020 EXPANDER



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.9	KEYBOARD AND POWER SUPPLY

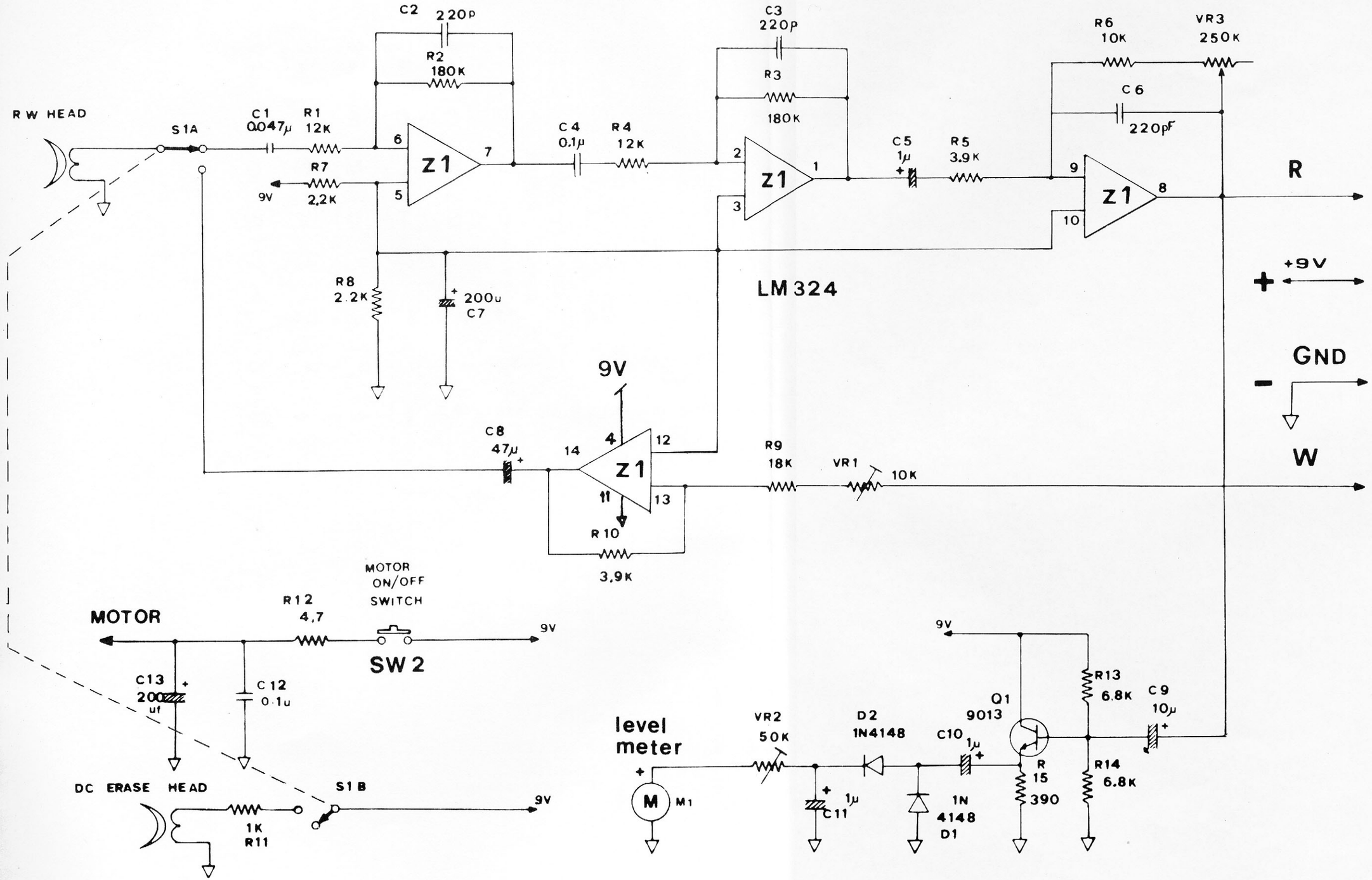


POWER SUPPLY

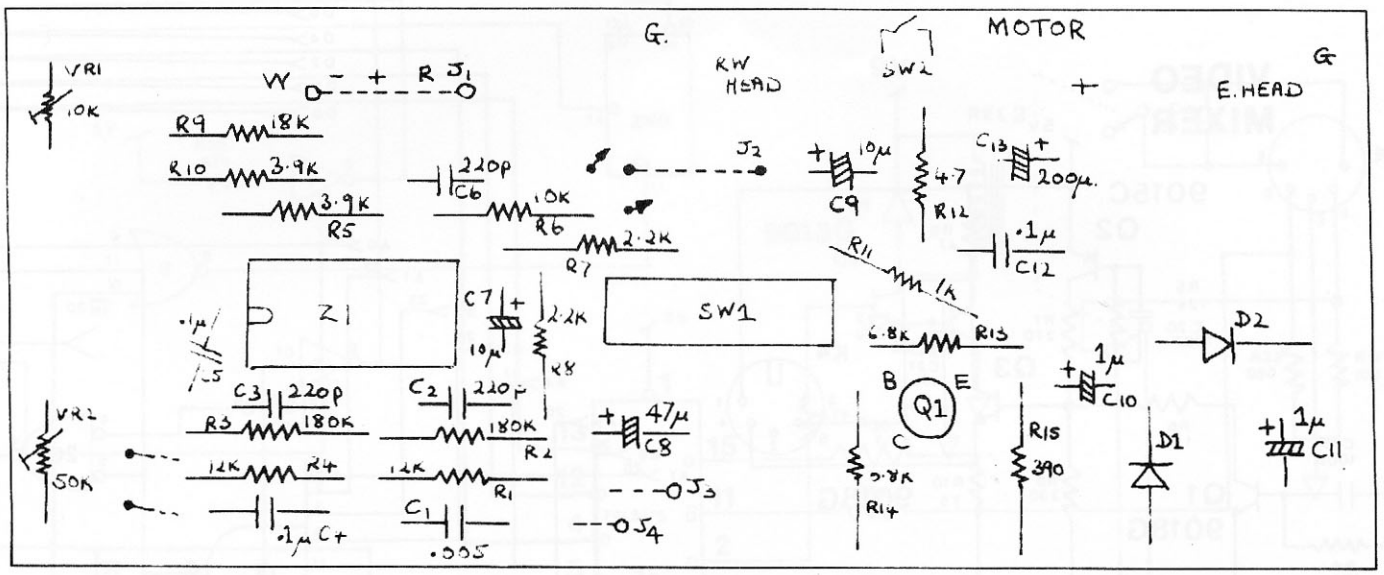


* Model 1 only
#Mk II only (function keys)

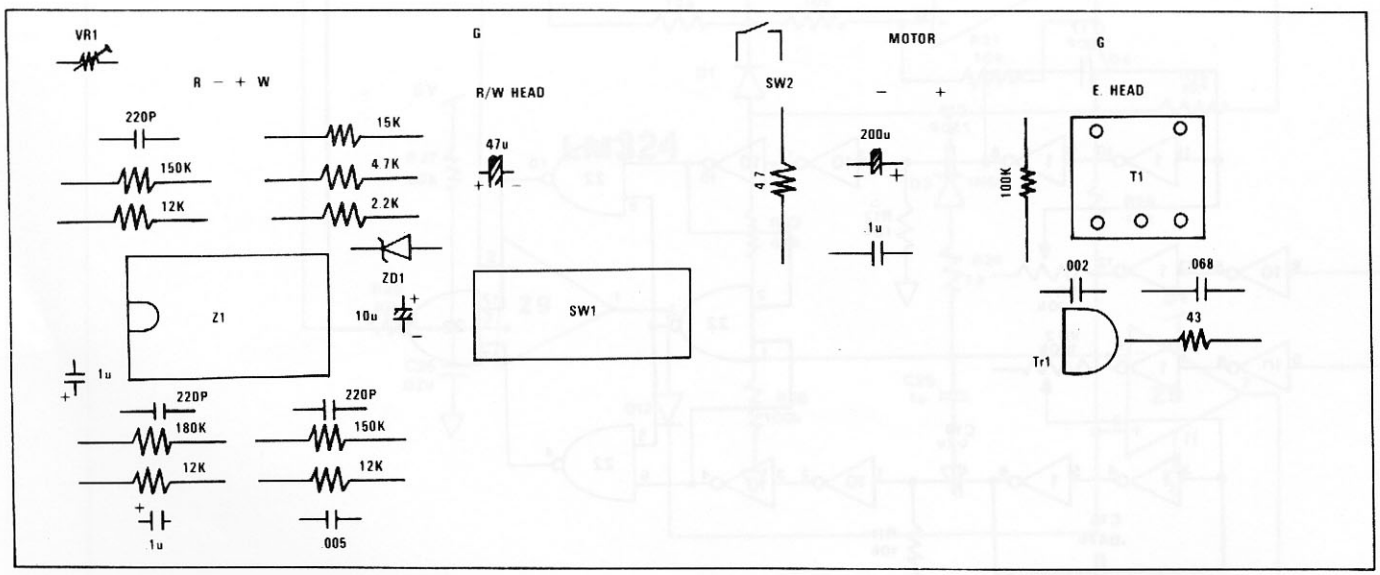
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.8	CASSETTE RECORDER



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.8	CASSETTE RECORDER



CASSETTE AMPLIFIER BOARD
(DC ERASE)

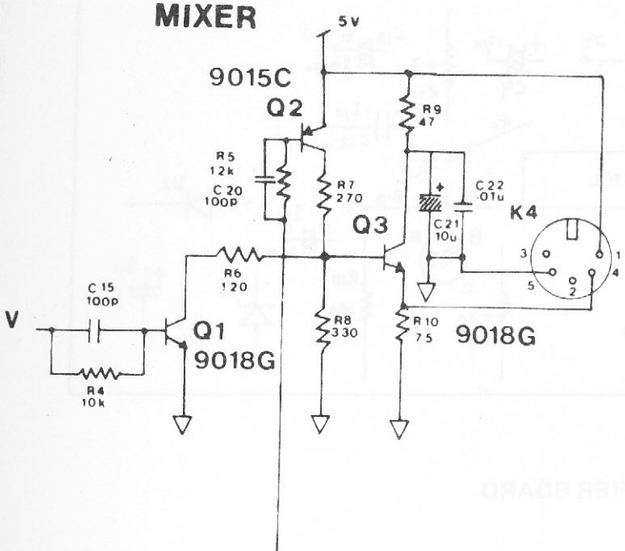


COMPONENT LAYOUT OF EACA P102 REV B

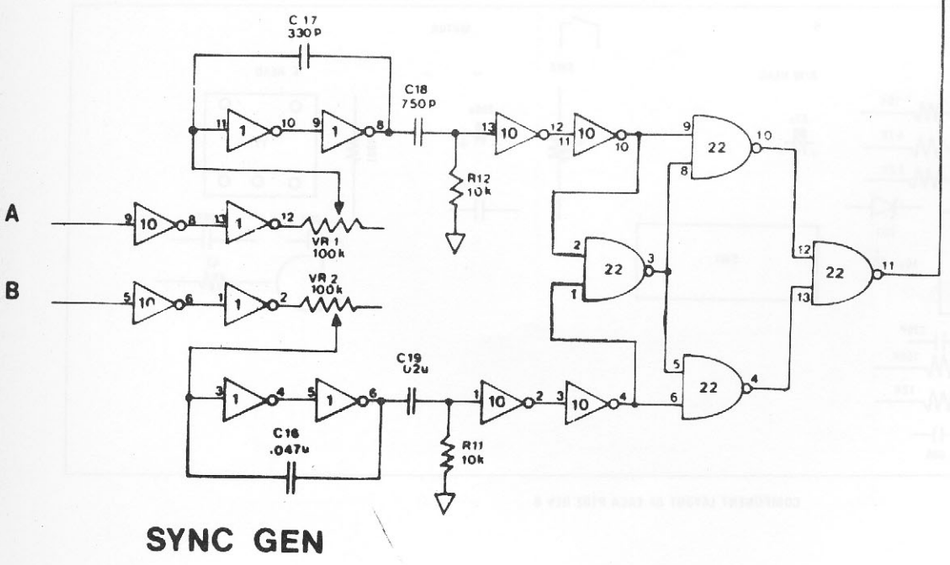
CASSETTE AMPLIFIER BOARD
(AC ERASE)

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.7	**CASSETTE INTERFACE** (Mk II) Note Blue Label models are fitted with speaker and associated components shown on preceding drawing (4.6)

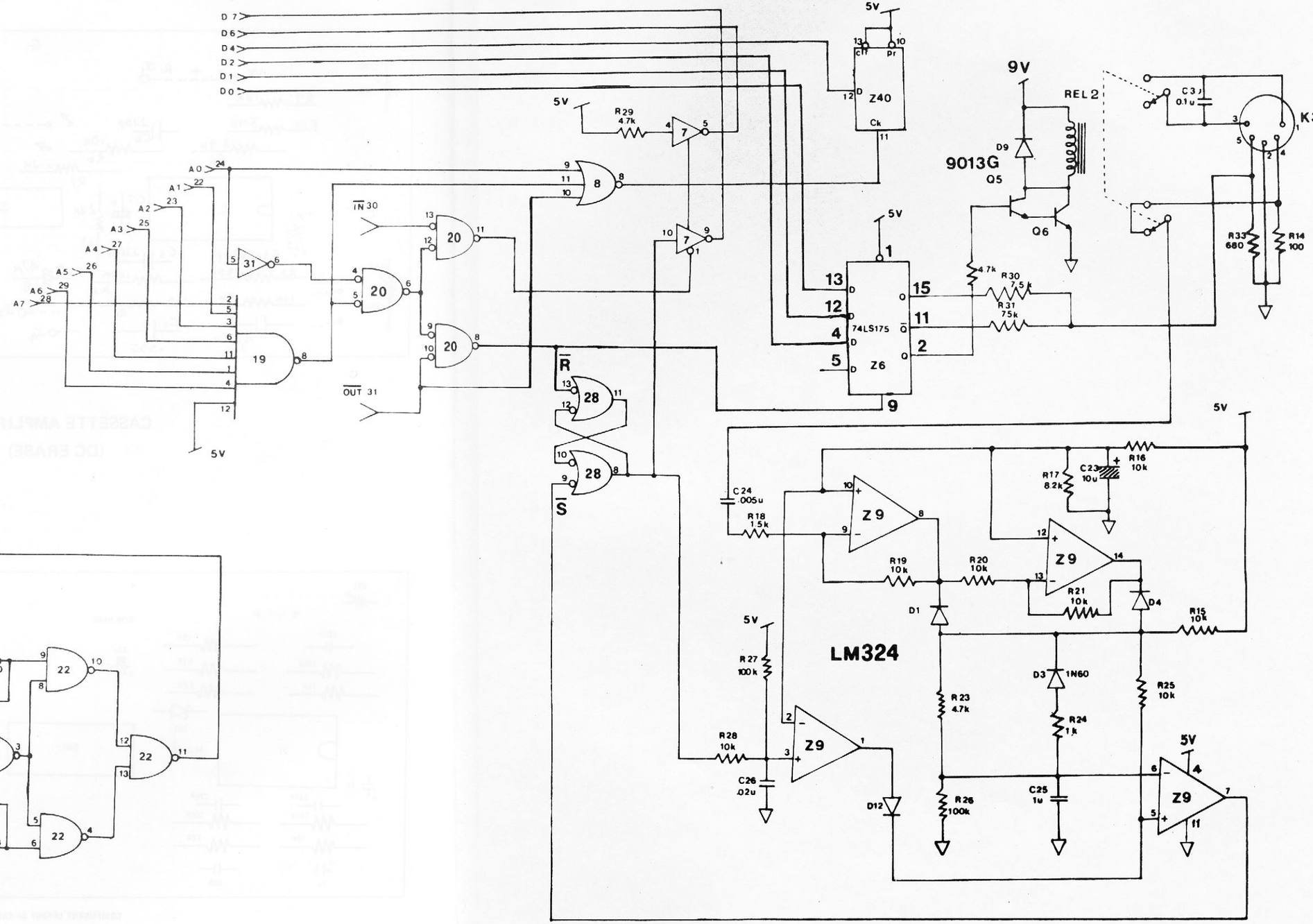
VIDEO MIXER



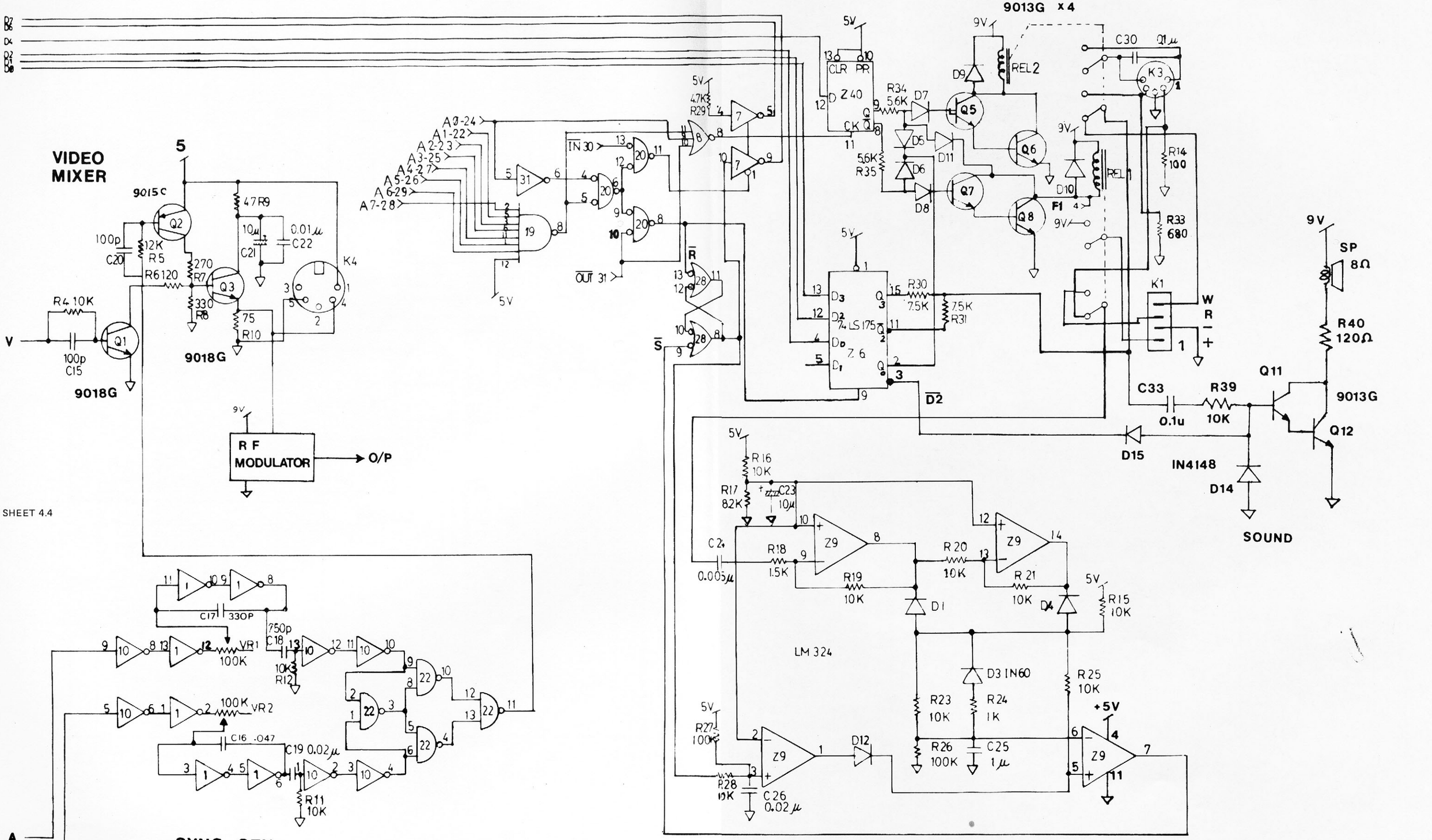
FROM SHEET 4.5

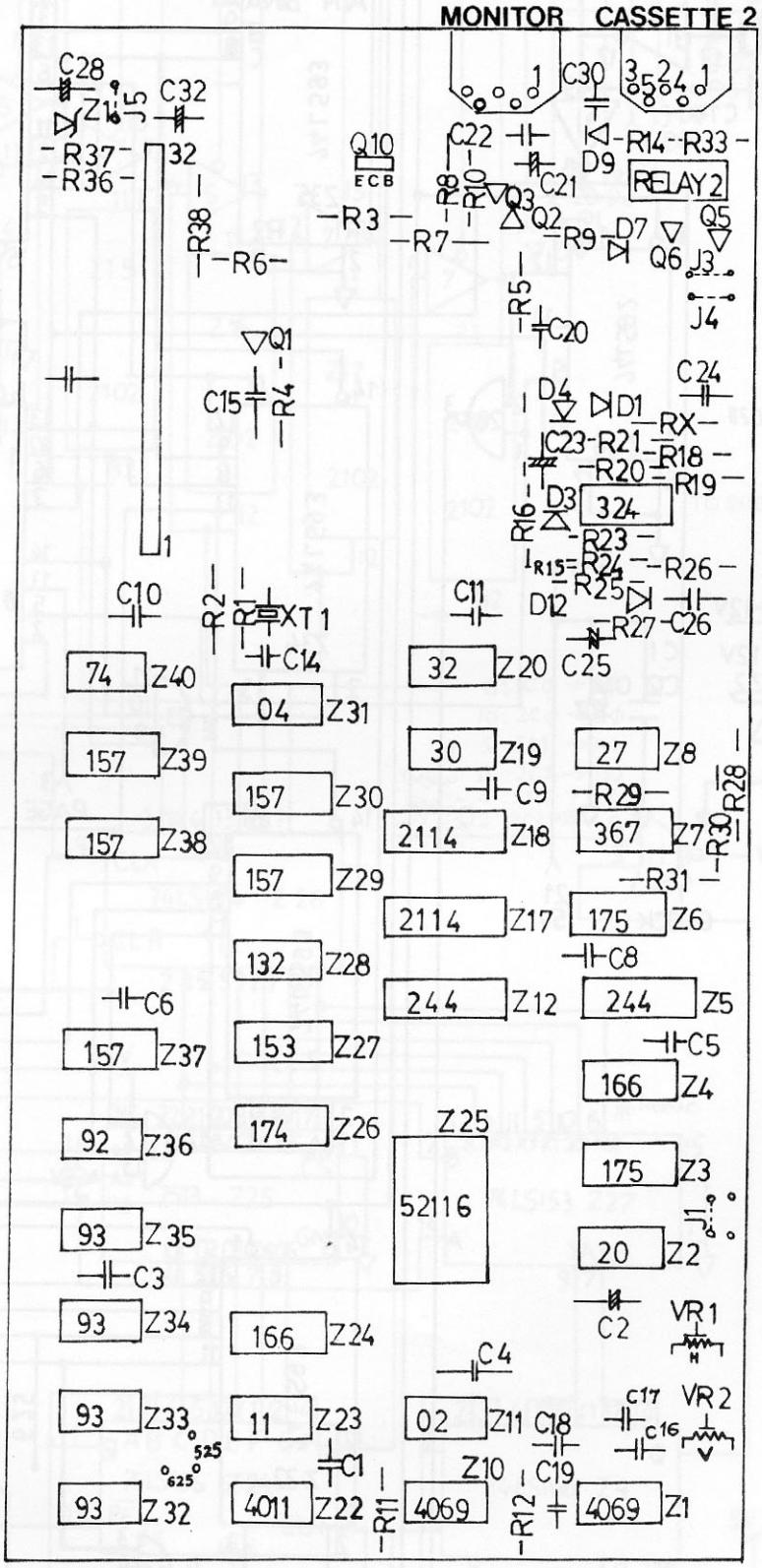


SYNC GEN



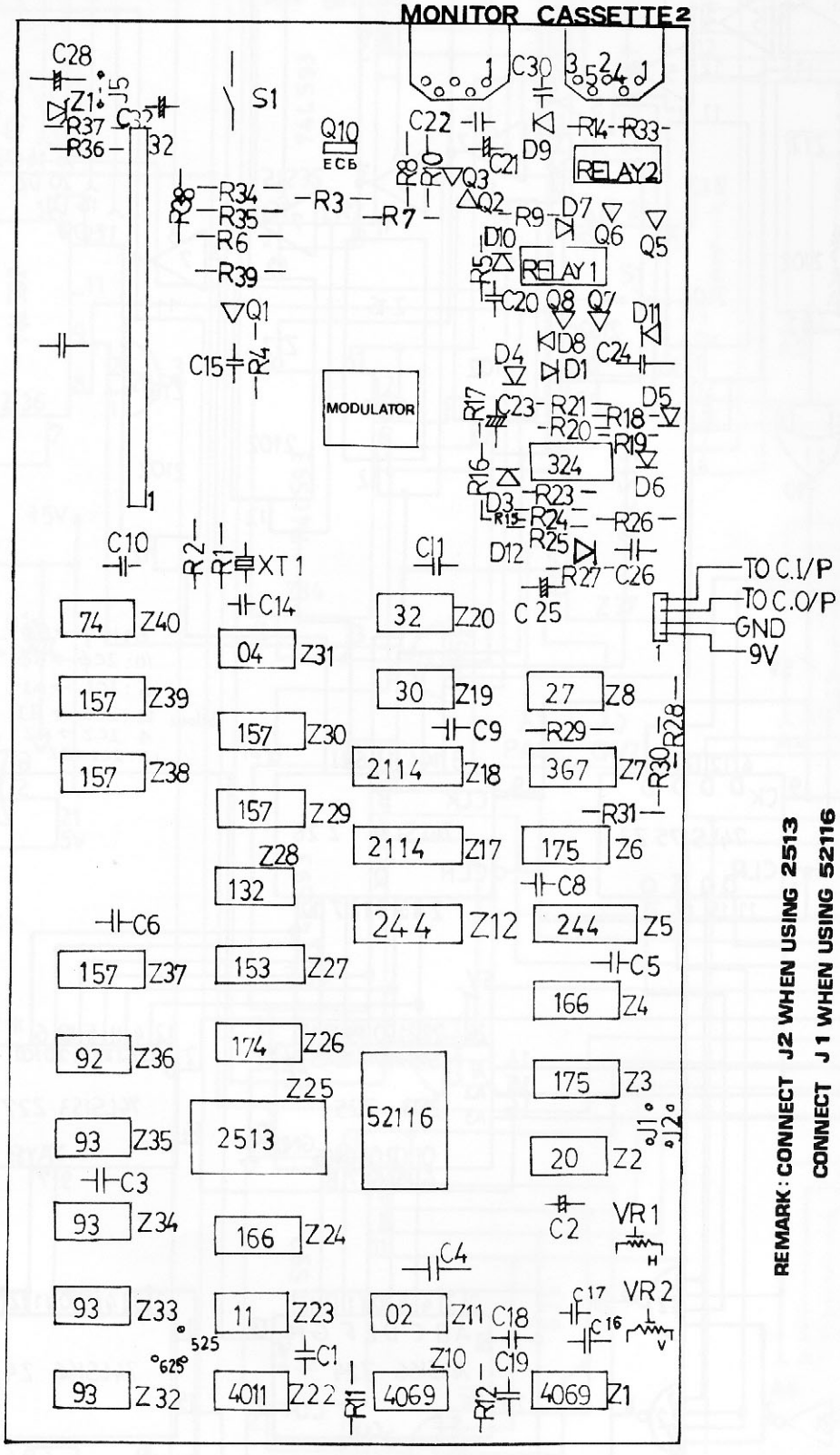
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.6	**CASSETTE INTERFACE** (Mk I) Note early models are not fitted with speaker and associated components





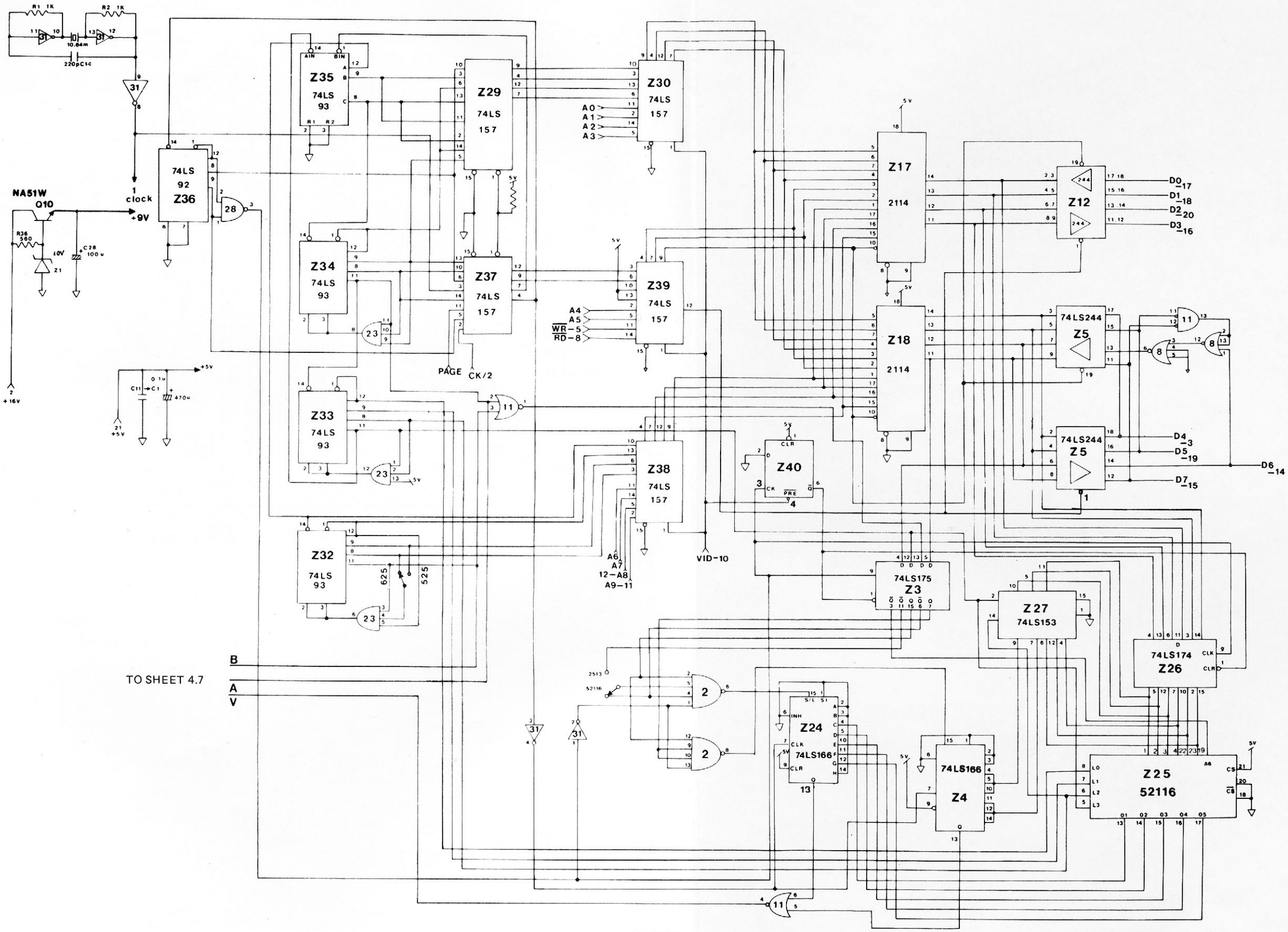
(Mk II Blue Label)

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.5	**VIDEO INTERFACE CARD** (Blue Label Series)

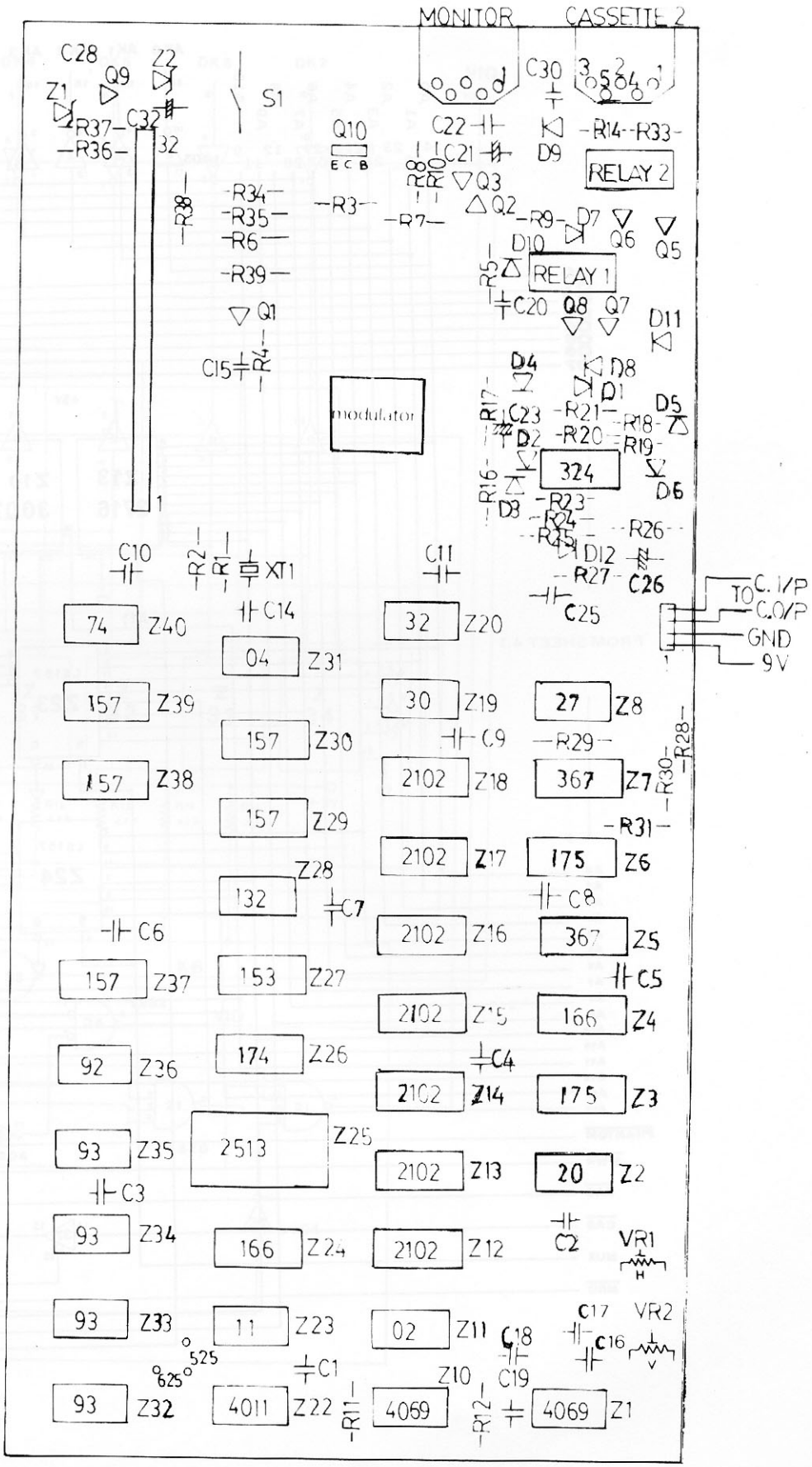


LATER Mk I

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.5	**VIDEO INTERFACE CARD** (Blue Label Series)



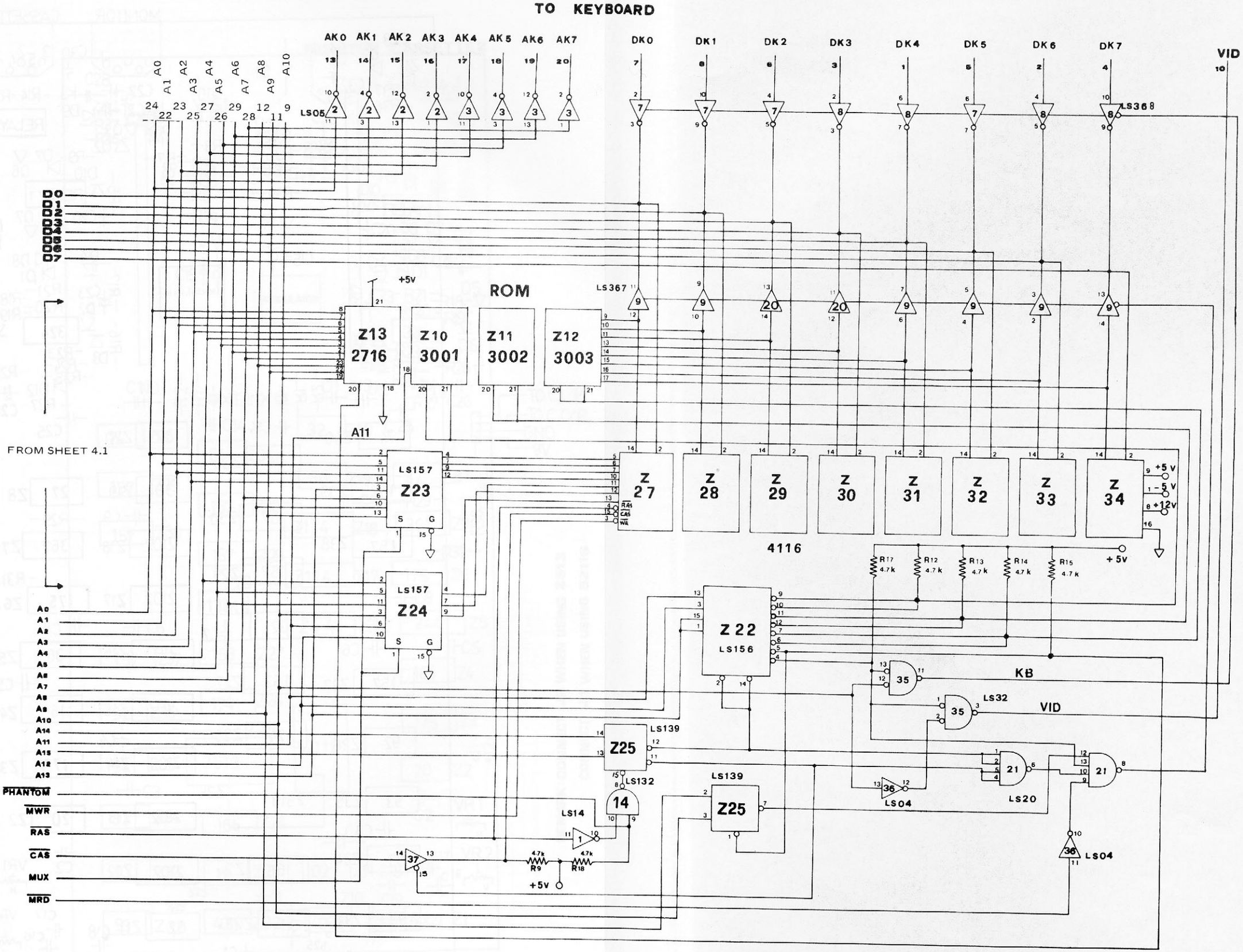
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.4	**VIDEO INTERFACE CARD** (Early Models)



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.4	VIDEO INTERFACE CARD (Early Models)

R1 1K
R2 1K
10·6495 MHz
220p C14
Q10
Q9
+9V
560 R37
1K R36
C28
8.2V Z1
R38 560
+12V
12V Z2
C32 10µ
C1
C12 01µ
0.01µ C33
C31
2 +16V
3 GND
1 CLOCK
21 5V
+5V
74LS92 Z36
74LS593 Z35
74LS593 Z34
74LS93 Z33
74LS93 Z32
74LS157 Z29
74LS157 Z37
74LS157 Z30
74LS157 Z39
74LS157 Z38
S1
R3 4.7K
5V
PAGE
CK/2
A0
A1
A2
A3
A4
A5
A6
A7
RD-8
WR-5
A9-11
A8-12
VID-10
525
525
Z12 2102
Z13 2102
Z14 2102
Z15 2102
Z16 2102
Z17 2102
Z18 2102
D7
D6
D4
D2
D1
D0
15-D7
14 D6
19-D5
13-D4
16-D3
20-D2
18-D1
17-D0
TO SHEET 4.6
CLR Z40
CK PRE Q
74LS175 Z3
74LS174 Z26
2513 Z25
74LS153 Z27
74LS166 Z24
74LS166 Z4
6 : 1Cφ → Aφ
10 : 2Cφ → Bφ
* 5 : 1C1 → A1
Below 11 : 2C1 → B1
4 : 1C2 → A2
12 : 2C2 → B2
*Above
A
B

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.3	CPU BOARD-2 MEMORY (MkII and Blue Label Series)



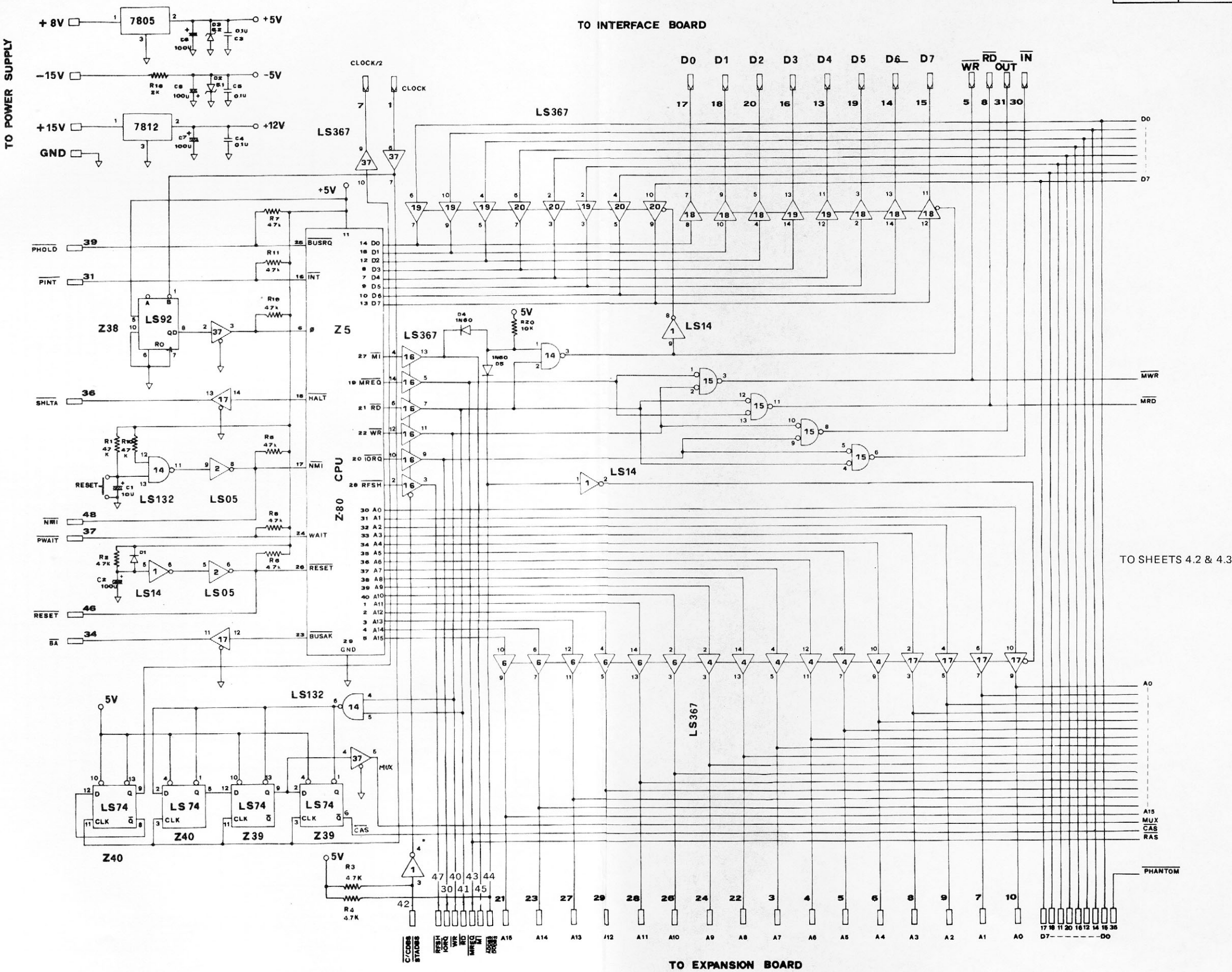
DICK SMITH SYSTEM 80	
DRAWING 4.2	*TITLE* CPU BOARD-2 MEMORY (Early Models)

TO KEYBOARD

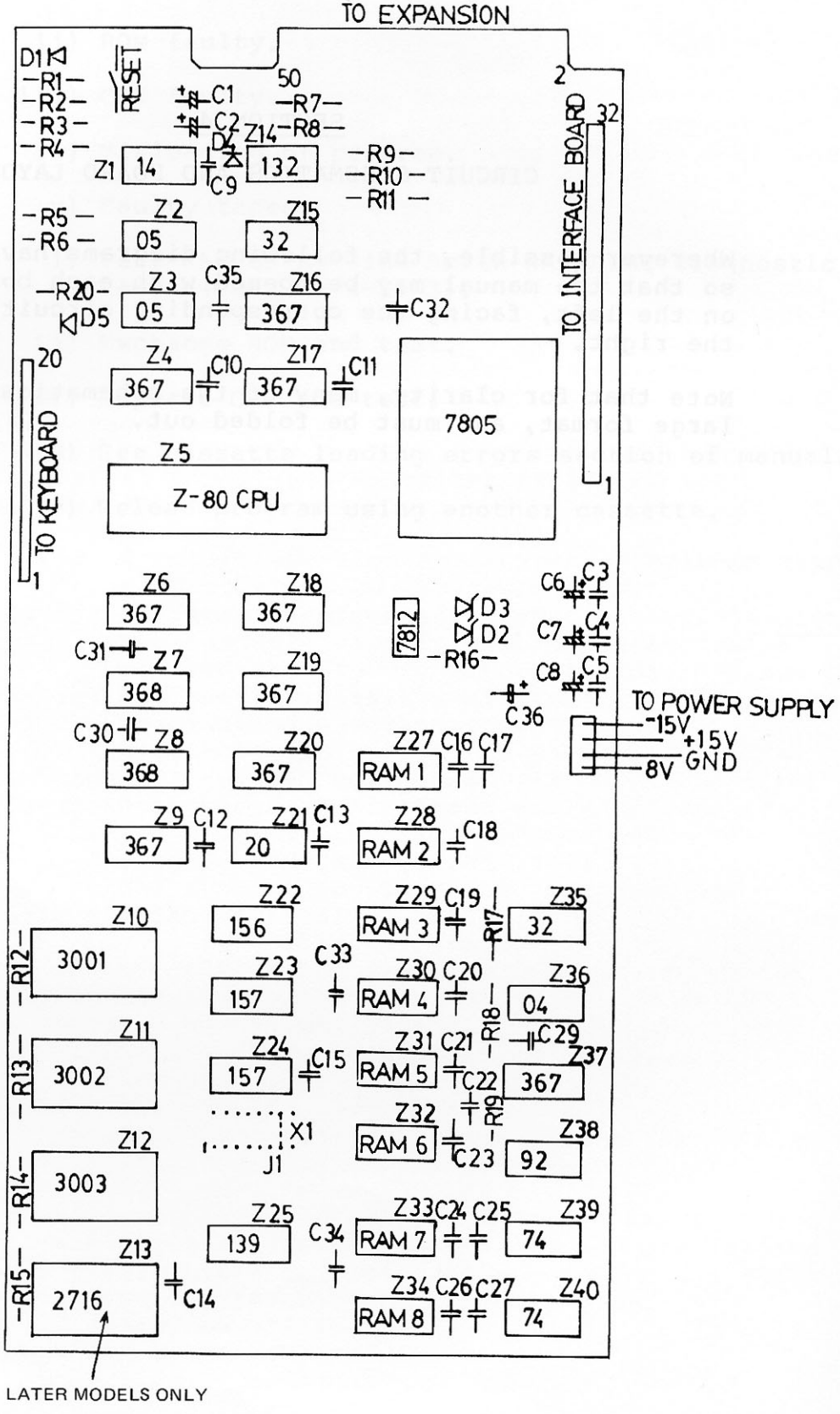
FROM SHEET 4.1

TO SHEET 4.3

DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.1	CPU BOARD (All Models)



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.1	**CPU BOARD** (All Models)



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.23	X-4013 PARALLEL PRINTER INTERFACE

50–PIN EDGE CONNECTOR
FROM SYSTEM 80

VCC 19 → +5V

GND1,2, 49,50 → GND

D7 17
D6 18
D5 11
D4 20
D3 16
D2 12
D1 14
D0 15
A1 7
A0 10
A2 9
A3 8
A4 6
A5 5
A6 4
A7 3
IORQ 38
RD 41
WR 40

Z7 74LS367

Z6 74LS175

Z5 74LS175

Z4a 74LS32

Z4b

Z3 74LS30

Z1a
Z1b
Z1c
Z1d
74LS32

Z2 a 74LS123

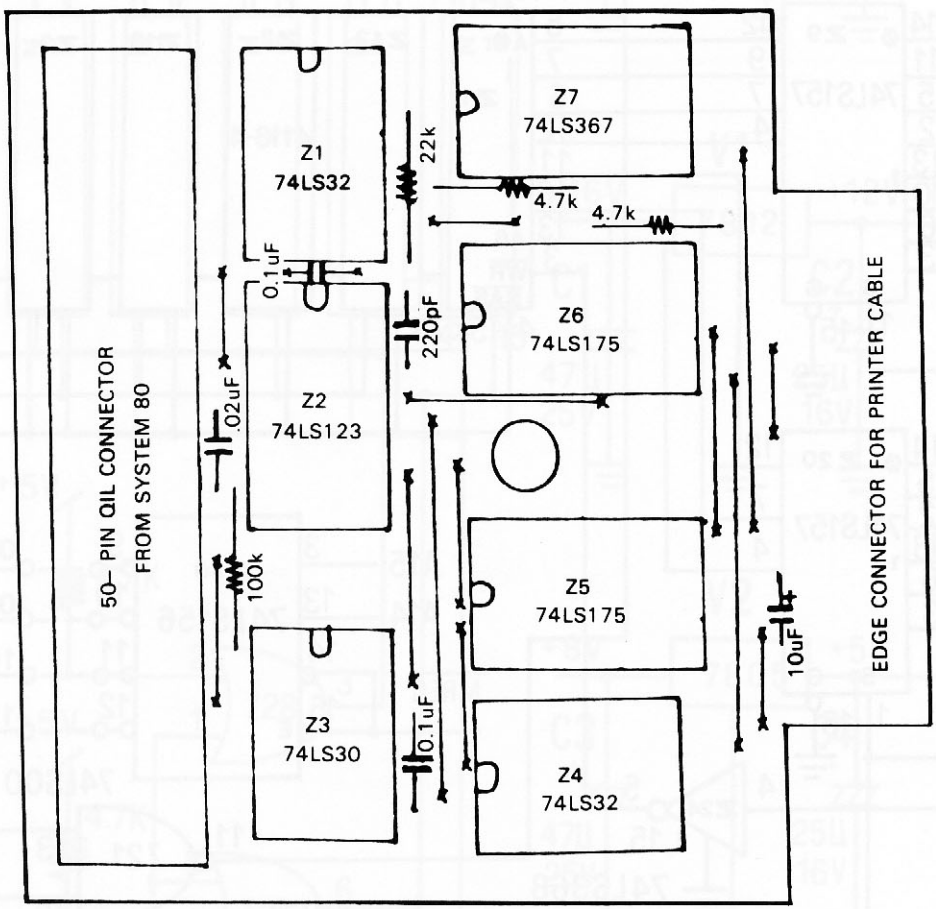
Z2b

5V
4.7k
4.7k
22k
220pF
100k
.02uF

36–PIN CONNECTOR FOR PRINTER

21 BUSY
23 OUTPAPER
25 UNIT SEL
28 $\overline{\text{FAULT}}$
17 DATA BIT 7
15 DATA BIT 6
13 DATA BIT 5
11 DATA BIT 4
9 DATA BIT 3
7 DATA BIT 2
5 DATA BIT 1
3 DATA BIT 0
1 $\overline{\text{DATA STROBE}}$
2,4,6,8,10,12,14, 16,18,20,22,24,27, 31 ALL GROUNDED
OTHERS NC

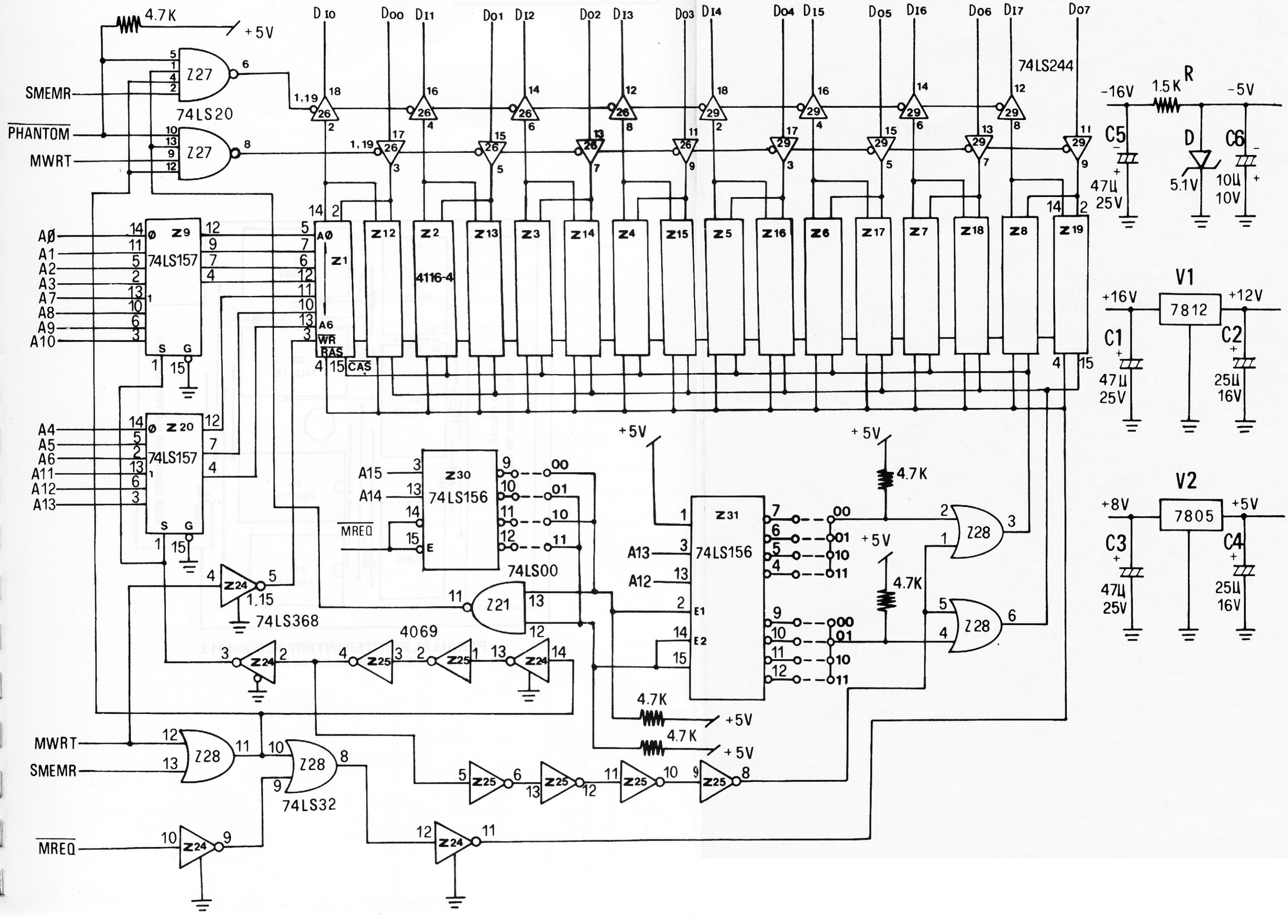
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.23	X-4013 PARALLEL PRINTER INTERFACE



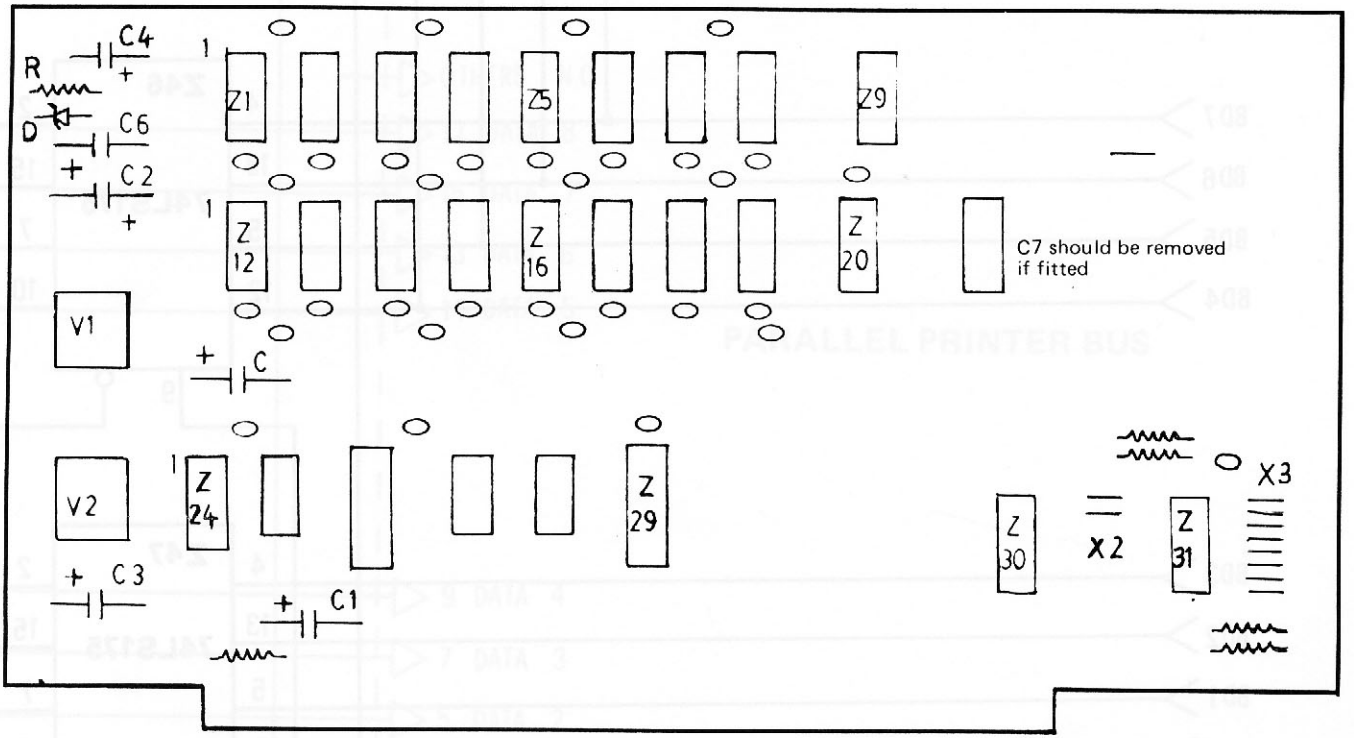
PARALLEL PRINTER INTERFACE X-4013

COMPONENT LAYOUT ON PCB

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.22	X-4016 RAM CARD



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.22	X-4016 RAM CARD



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.21	X-4010 EXPANSION UNIT PARALLEL PRINTER PORT

+5V

R18
4.7K

74LS32

Z48

Z50
74LS244

Z46
74LS175

Z47
74LS175

Z49
74LS123

Z56

74LS00

74LS32

C10 .02µ R16 100K

C11 470P R17 20K

BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0

$\overline{BRD}$
$\overline{PPR}$
$\overline{SPR}$
$\overline{BWR}$

21 BUSY
23 OUTPAPER
25 UNIT SEL
2.4.6.8.10.12.14.16.18.20.22.24 GND
OTHERS N.C.
17 DATA 8
15 DATA 7
13 DATA 6
11 DATA 5
9 DATA 4
7 DATA 3
5 DATA 2
3 DATA 1
1 $\overline{DATA\ STRB}$

PARALLEL PRINTER BUS

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.20	X-4010 EXPANSION UNIT RS-232C COMMUNICATIONS PORT

+5V

R37-41
4.7K

DP1

UART
Z54

1 PGND
7 SGND
2 TXD
3 RXD
8 CD
6 DSR
5 CTS
20 DTR
4 RTS

RS232 BUS

1488
Z53

1489
Z57

74LS132
Z56

SRESET

74LS244
Z51

74LS244
Z50

R33
1.5M
3.579MHz
C12 30P
C13 30P
4069
Z60

R34 47K
R35 47K

R36
1K

74LS30
Z59

9015
C14
470P

DP2

74LS93
Z58

4520
Z61

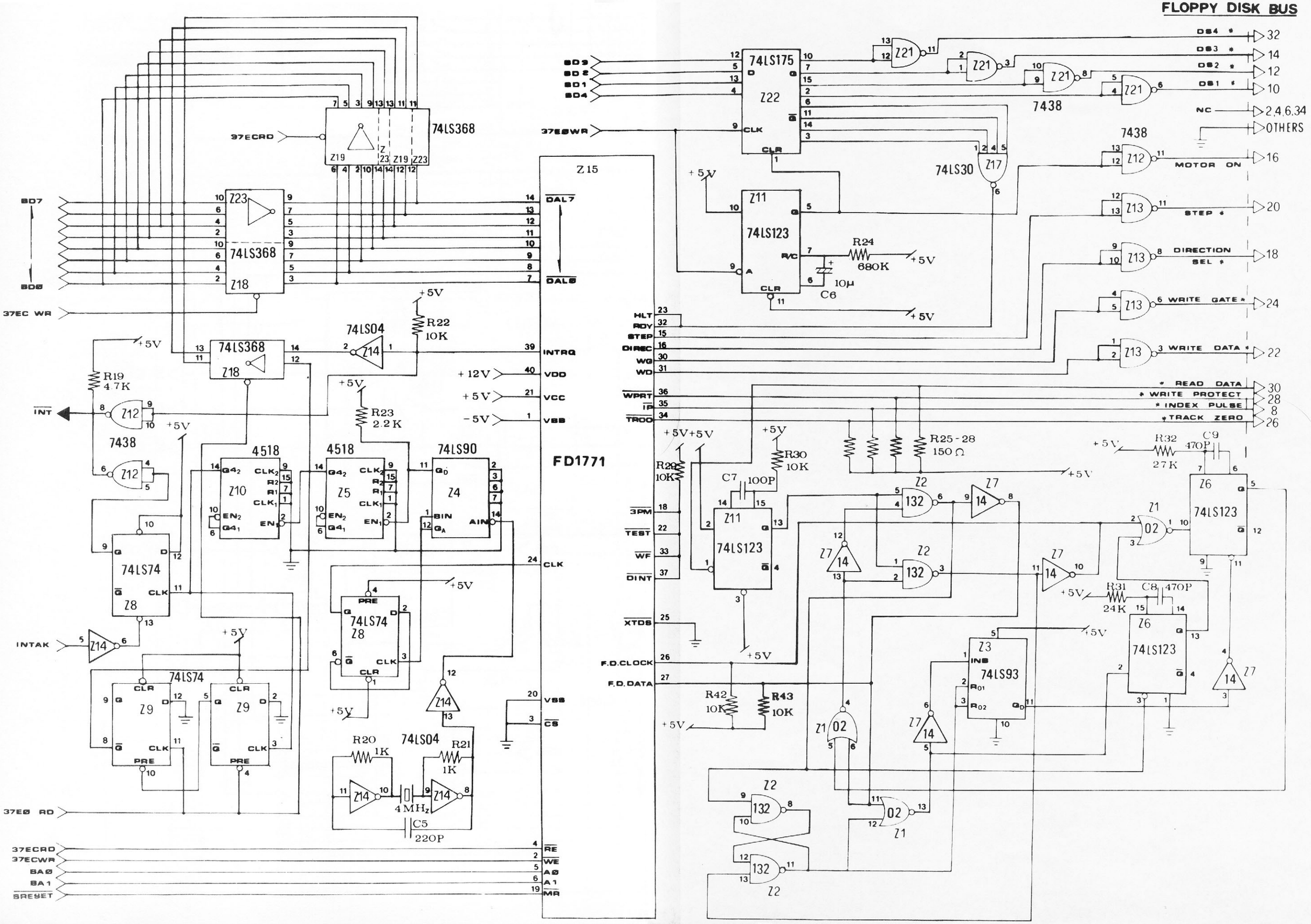
74LS175
Z52

74LS00
Z56

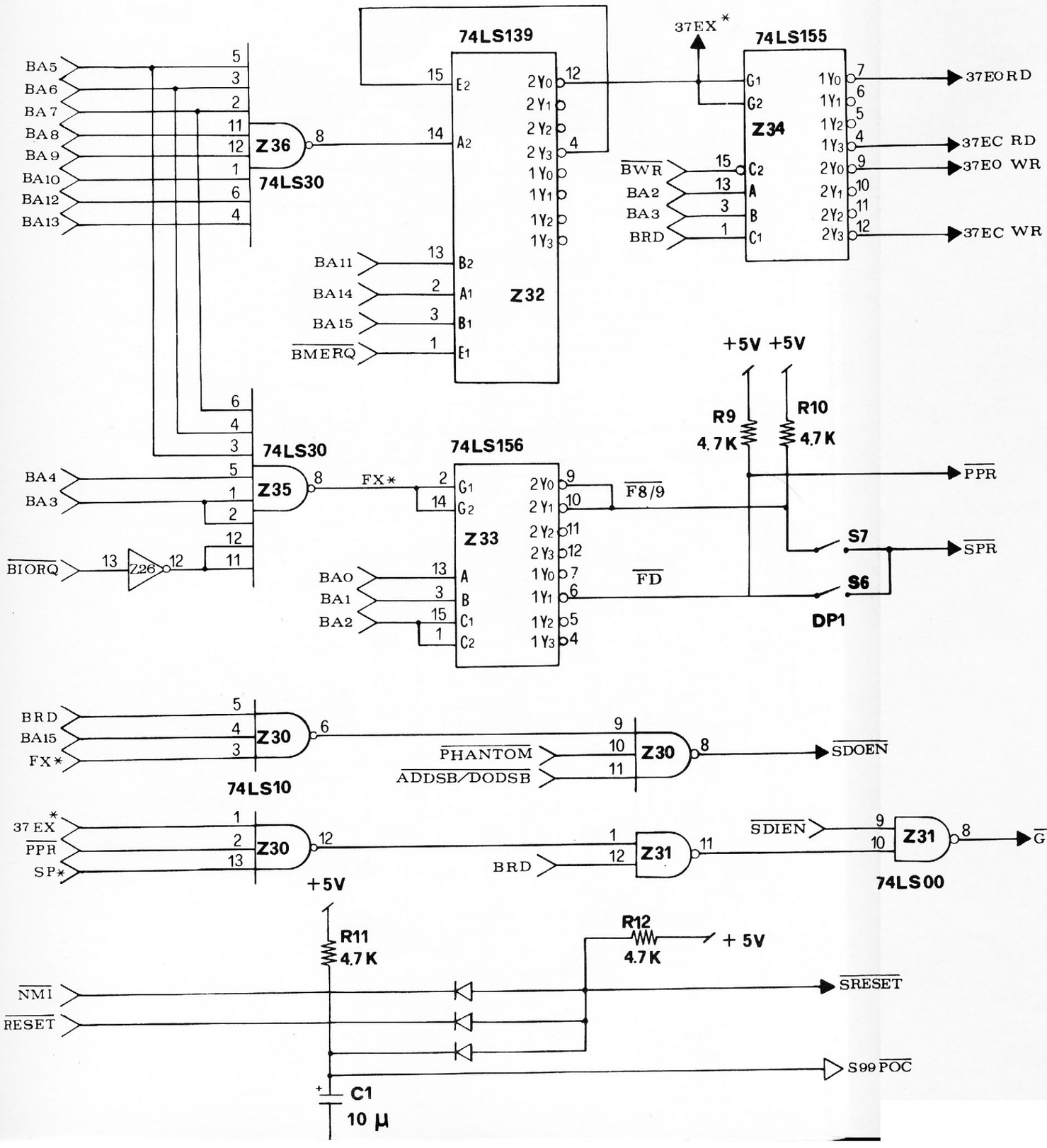
74LS138
Z55

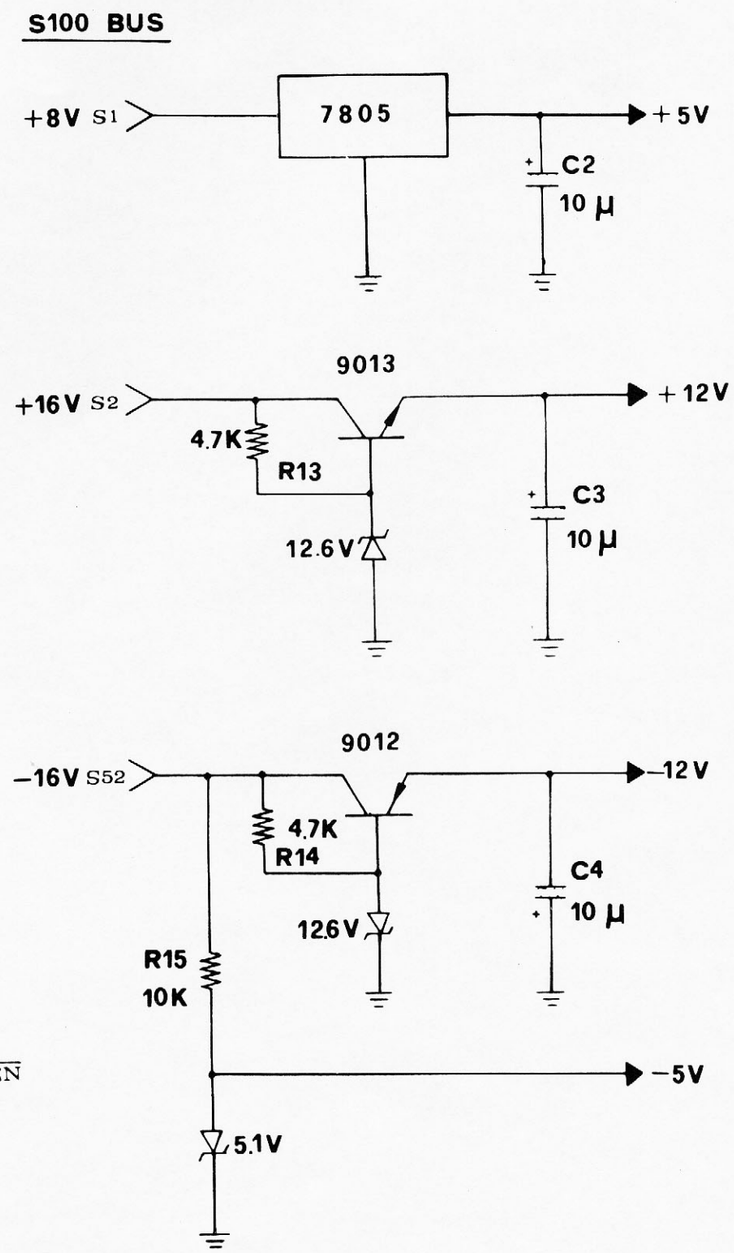
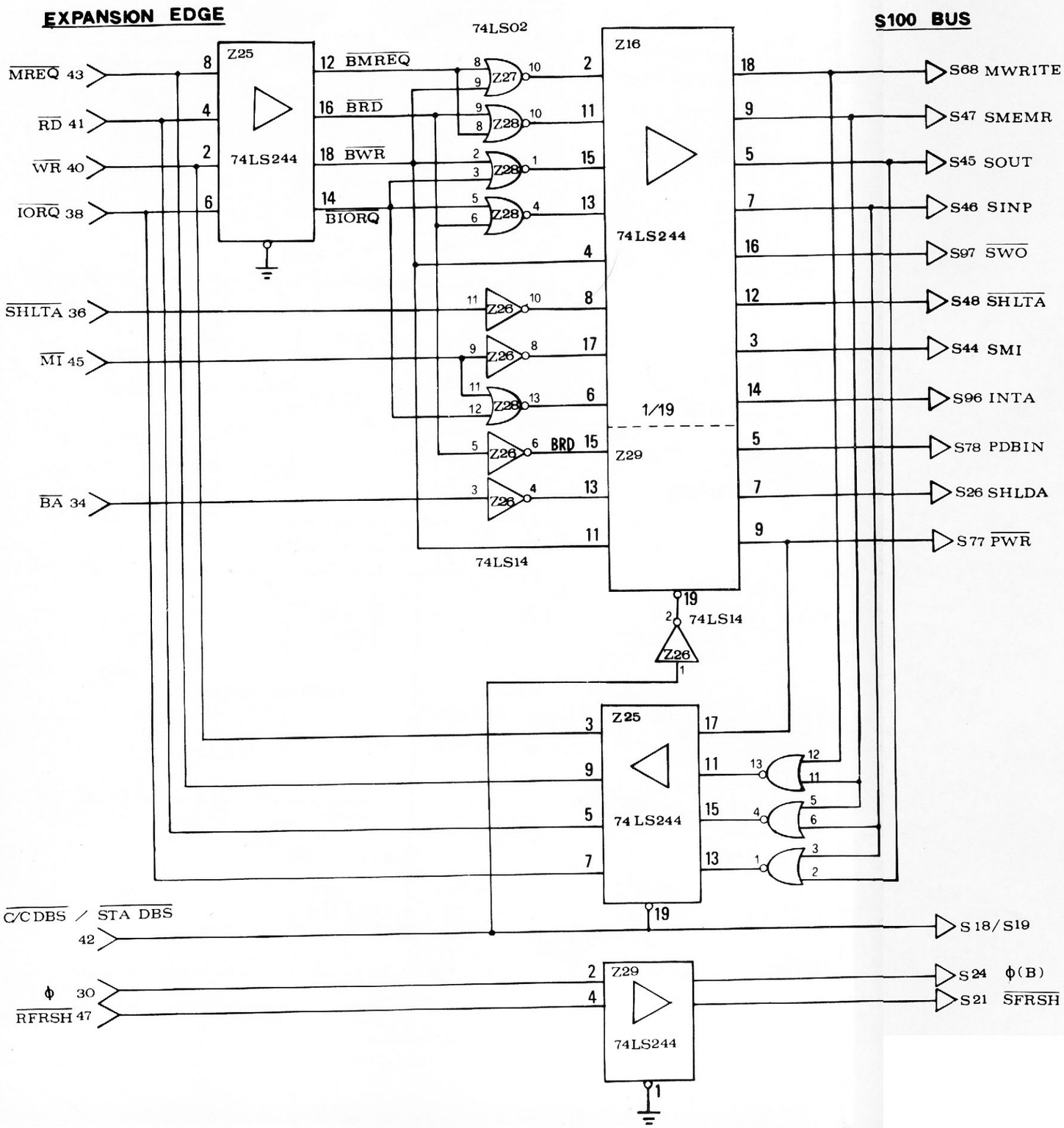
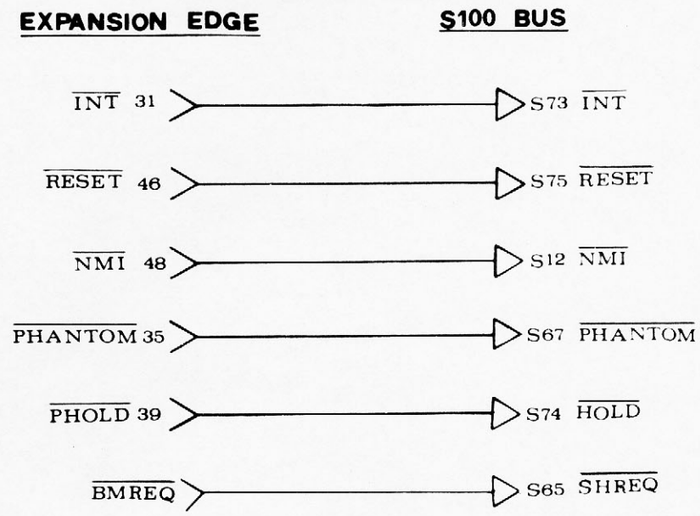
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.19	X-4010 EXPANSION UNIT FLOPPY DISK CONTROLLER

FLOPPY DISK BUS



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.18	X-4010 EXPANSION UNIT ADDRESS DECODING





DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.17	X-4010 EXPANSION UNIT S100 INTERFACE